MODELING AND SIMULATION OF THE EFFECTS OF THERMAL EXPANSION MISMATCH AND TEMPERATURE ON THERMAL INDUCED STRESSES IN MODERN NANO PMOS

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ABSTRACT

Stress is used to enhance dramatically the electrical and optical performances of modern nanotransistors and solar cells. The purpose of this paper is to develop and apply accurate mathematical models to simulate and analyze correctly the thermal induced stresses in nano pMOS transistors having Silicon-Germanium (SiGe) thin films as stressors. These stresses are due to the growth temperatures of the SiGe films and to the thermal mismatch between the thermal expansion coefficients (TECs) of SiGe films and Silicon substrate. In the proposed models, we are accurately taking into account the effects of the fabrication temperatures on the TECs of SiGe films and Silicon substrate to calculate the resulting thermal strains and stresses. Numerical results showing the effects of growth temperatures and thermal mismatch between TECs of SiGe and Silicon on the resulting thermal stresses will be presented, discussed and compered with literature for Intel 14 nm pMOS transistor.

Keywords: Growth temperature effects, thermal expansion mismatch effects, modeling thermal induced stresses ,Intel 14 nm nano pMOS transistors

1. INTRODUCTION

Nano pMOS and nMOS transistors are the backbone of today's economy. They have many applications in our daily life. They are used in the RAMs, CPUs, and GPUs of any new laptops, smart phones, tablets, or in solar cells. They are also used in the new generation of iPad and smart-phone touch screens, or light-emitting diode displays for televisions, mobile phones, and computer monitors. Nanotransistors provide high performance, lower power consumption, lower cost per transistor and high level of integration compared to the micro transistors used between the invention of the first transistor in 1945 and the year 2000. The first nanotransistors were mainly born in the beginning of the year 2000. For example, Intel's Core i3 and i5 CPUs, released in January 2010, were among the first mass-produced processors to use nanotransistors with 32 nm technology node.

In February 2015, Samsung announced that its flagship smartphones Galaxy S6 and Galaxy S6 Edge would use nanotransistors with 14 nm technology node. Nanotransistors based on Graphene material are the new candidates for the next generation solar cell applications and photovoltaic industry (Yin et al., 2014).

Since 2004, the leading manufacturers of nano pMOS and nMOS transistors as Intel, IBM and Samsung have been using intentionally material mismatch stress and thermal mismatch stress to enhance dramatically the mobility and speed of the new generation of nanotransistors. It has been shown in (Moroz et al., 2006) that the application of a compressive stress originating from different stressors enhanced the mobility of holes in nano pMOS transistors by 200%.

Intel technology is using epitaxy method and high temperatures T to grow Silicon-Germanium (Si(1-x)Ge(x)) thin film pockets in source and drain of nano pMOS to introduce intentionally a compressive extrinsic stress σ in the channel (Moroz et al., 2004, 2005, 2006, 2012, 2013; Bera et al., 2006; Chui et al., 2007). This compressive extrinsic stress σ is due mainly to an intrinsic (i.e. initial) compressive stress σ_0 which is generated in Si(1-x)Ge(x) thin films after their growth on Silicon (Si) at elevated temperatures T. This intrinsic stress σ_0 is the sum of the initial stresses σ_0^{mm} and $\sigma_0^{tm}(T)$. Where, σ_0^{mm} is due to the lattice mismatch between Si(1-x)Ge(x) films and Silicon substrate. And, $\sigma_0^{tm}(T)$ is the initial thermal mismatch stress due to the thermal mismatch between the TECs of Si(1-x)Ge(x) thin films and Silicon substrate and to the change of temperature from the growth temperature T to the room temperature T0. In this paper, we are ignoring σ_0^{mm} and focusing on the study of the initial thermal mismatch stress $\sigma_0^{tm}(T)$ and the resulting extrinsic thermal mismatch stress σ.

Let $\Delta\alpha(x,T) = -\alpha_{Si(1-x)Ge(x)}(T) + \alpha_{Si}(T)$ represents the thermal expansion mismatch between the thermal expansion coefficient $\alpha_{Si(1-x)Ge(x)}(T)$ of Si(1-x)Ge(x) thin films and the thermal expansion coefficient $\alpha_{Si}(T)$ of Silicon substrate. And, let $\Delta T = T - T0$ represents the change in temperature. T0 is the room temperature.

We assume that Silicon, Germanium, and Si(1-x)Ge(x) are elastic materials. In this case, we can use Hooke's law to calculate the initial thermal induced stress tensor $\sigma_0^{tm}(T)$:

$$\sigma_0^{tm}(T) = (\sigma_0^{xx}(T), \sigma_0^{yy}(T), \sigma_0^{zz}(T), \sigma_0^{xy}(T), \sigma_0^{yz}(T), \sigma_0^{xz}(T))$$

in terms of the initial thermal induced strain tensor $\varepsilon_0^{tm}(T)$:

$$\varepsilon_0^{tm}(T) = (\varepsilon_0^{xx}(T), \varepsilon_0^{yy}(T), \varepsilon_0^{zz}(T), \varepsilon_0^{xy}(T), \varepsilon_0^{yz}(T), \varepsilon_0^{xz}(T))$$

as follows:

$$\sigma_0^{tm}(T) = D\varepsilon_0^{tm}(T), \quad (1)$$

where D represents the 6 by 6 stiffness matrix. It is calculated from the elastic constants c11, c12, and c44 as in (El Boukili, 2010). The terms $\sigma_0^{xx}(T), \sigma_0^{yy}(T), \sigma_0^{zz}(T)$ are the initial normal stress components. And, $\sigma_0^{xy}(T), \sigma_0^{yz}(T), \sigma_0^{xz}(T)$ are the initial shear stress components. The terms $\varepsilon_0^{xx}(T), \varepsilon_0^{yy}(T), \varepsilon_0^{zz}(T)$ are the initial normal strain components. And, $\varepsilon_0^{xy}(T), \varepsilon_0^{yz}(T), \varepsilon_0^{xz}(T)$ are the initial shear strain components.

We could see from Equation (1) that to calculate correctly and accurately the initial thermal stress $\sigma_0^{tm}(T)$ in Si(1-x)Ge(x) thin films, we need to calculate correctly and accurately the initial thermal mismatch strain $\varepsilon_0^{tm}(T)$.

The initial thermal mismatch strain $\varepsilon_0^{tm}(T)$ is calculated from the thermal expansion coefficients $\alpha_{Si(1-x)Ge(x)}(T)$, $\alpha_{Si}(T)$, and $\alpha_{Ge}(T)$ of Si(1-x)Ge(x) thin films, Silicon (Si), and Germanium (Ge) respectively.

There are three levels of originalities in this paper. The first originality is to propose and apply an accurate and physically based model to calculate accurately the TECs $\alpha_{Si(1-x)Ge(x)}(T)$, $\alpha_{Si}(T)$, and $\alpha_{Ge}(T)$ under the effects of the fabrication temperatures T and Ge mole fraction x.
The second originality is to propose and apply new and accurate physically based model to calculate accurately the thermal induced initial strain $\varepsilon_0^{tm}(T)$ and stress $\sigma_0^{tm}(T)$. The third originality is to proposed and apply new and accurate physically based model to calculate the thermal induced extrinsic stress σ from $\sigma_0^{tm}(T)$ using Finite Volumes method in the whole structure of Intel 14 nm nano pMOS transistor.

The investigation, analysis, and quantification of the effects of the thermal expansion mismatch represented by $\Delta\alpha(x,T)$ and the change in growth temperatures T on the resulting thermal extrinsic stress σ will be presented and discussed. This analysis will show to us how much thermal stress σ we will get when we change $\Delta\alpha(x,T)$ and ΔT. And, if we know how much thermal stress we get, we will know by how much the speed performance of the nano pMOS will increase. Since the speed of nano pMOS increases with increasing hole mobility. And, the hole mobility increases with decreasing compressive stress σ according to (JianLi et al., 2014; Kumar et al., 2012). For example, it has been shown in (Moroz et al., 2006) that the application of a compressive stress increased the hole mobility by 200%. So, this analysis is of great importance to the manufacturers, engineers, and designers of modern nanotransistors.

And, it is also of great importance to the researchers and designers of the modern concentrators photovoltaic (CPV) solar cells or just Silicon based (SB) solar cells working in arid regions where the temperature is high as the desert of Morocco or elsewhere. Since the thermal induced tensile stresses will reduce the efficiency of the CPV (or SB) solar cells.

This paper is organized as follows. Section 2 presents the main different sources of initial stress. Section 3 will present the proposed model to calculate the TECs $\alpha_{Si(1-x)Ge(x)}(T)$ and $\alpha_{Si}(T)$ under the effects of the fabrication temperatures T. Section 4 will outline the proposed new and physically based models to calculate the thermal induced intrinsic and extrinsic stresses ($\sigma_0^{tm}(T)$ and σ). Section 5 will present the numerical results for the resulting thermal induced

stress σ . It will present the validation and comparison of these results with experiments from literature. It will also present a quantitative and qualitative analysis of the effects of the thermal expansion mismatch $\Delta\alpha(x,T)$ and the change in the fabrication temperatures ΔT on the thermal induced stresses σ in Intel 14 nm nano pMOS transistors. Section 6 presents the concluding thoughts and future work.

2. DIFFERENT SOURCES OF INITIAL STRESS

The initial stress σ_0 in the Si(1-x)Ge(x) thin films or in the Silicon substrate depends on many different types of sources as: deposition, oxidation, etching, shallow trench isolation, diffusion, implantation, and neighboring. After deposition, two types of initial stresses will be created in the Si(1-x)Ge(x) thin films: the initial stress due to the lattice mismatch between Si(1-x)Ge(x) and Silicon materials. And, the initial stress due to thermal mismatch. The initial stress σ_0 due to lattice mismatch has been investigated in our previous work (El Boukili 2010). In this paper, we are going to focus on the modeling and analysis of the initial stress σ_0 induced by thermal mismatch.

2.1. Initial stress due to lattice mismatch

Right after deposition, thin films are either stretched or compressed to fit the substrate on which they are deposited. The film wants to be smaller if it was stretched earlier, thus creating a tensile initial stress. And, similarly, it creates a compressive initial stress if it was compressed during deposition. The initial stress generated due to this phenomenon can be quantified by Stoney's equation which relates the stress σ_0 to the substrate curvature or by other advanced models (El Boukili 2010).

2.2. Intrinsic stress due to thermal mismatch

Thermal mismatch stress depends on the mechanical properties of the materials. It occurs when two materials with different coefficients of thermal expansion are heated or cooled down. When two different materials are heated or cooled down, they will expand or contract at different rates. During thermal processing, thin film materials like Si(1-x)Ge(x), Poly-Silicon, Silicon Dioxide, or Silicon Nitride expand and contract at different rates compared to the Silicon substrate according to their thermal expansion coefficients. This creates an initial thermal mismatch strain and stress in the film and also in the substrate. The deposition takes place at elevated temperatures. When the temperature is decreased from the fabrication temperature T to the room temperature T0, the volumes of the grains of Si(1-x)Ge(x) films and Silicon substrate shrink and the thermal stresses in the material increase. The initial thermal stress σ_0 in the Si(1-x)Ge(x) films depend mainly on the fabrication temperature T, the TECs of Si(1-x)Ge(x), Germanium ratio x, the substrate orientation, the doping, and the deposition technique used. For the current nano pMOS transistors, Si(1-x)Ge(x) films are grown using low pressure chemical vapor deposition (LPCVD), plasma enhanced chemical vapor deposition (PECVD), or Epitaxy. Intel company is using Epitaxial growth for Si(1-x)Ge(x) films.

3. MODELING OF TEMPERATURE EFFECTS ON TECS OF SI AND SIGE

To take into account the effects of the fabrication temperatures T on the TECs of Silicon, Germanium, and Si(1-x)Ge(x) thin films, we are proposing and applying the following models:

$$\alpha_{Si}(T) = s1.(1-\exp(-s2.(\frac{T^2}{s3}-s4))) + s5.T \qquad (2)$$

$$\alpha_{Ge}(T) = a1.(1-\exp(-a2.(\frac{T^2}{a3}-a4))) + a5.T \qquad (3)$$

$$\alpha_{Si(1-x)Ge(x)}(T) = (1-x)\alpha_{Si}(T) + x\alpha_{Ge}(T) \qquad (4)$$

The parameters s1, s2, s3, s4, s5, a1, a2, a3, a4, and a5 have been calculated, using the nonlinear least squares method, from fitting the models (2), (3), and (4) with experimental data found in (Okaji et al., 2004; Singh , 1968). The models (3)-(5) are accurate and fit excellently well with the experimental data from (Okaji et al., 2004; Singh , 1968).

4. NEW AND ACCURATE MODLS FOR THERMAL MISMATCH INDUCED INTRINSIC AND EXTRINSIC STRESSES

To take into account the effects of the fabrication temperatures T, the thermal mismatch $\Delta\alpha(x,T)$, and the Germanium content x on the thermal mismatch induced intrinsic strain $\varepsilon_0^{tm}(T)$ in the Si(1-x)Ge(x) thin films, we propose and apply the following accurate and physically based models:

$$\varepsilon_0(T) = \int_{T0}^{T} \Delta\alpha(x,t)dt\,. \qquad (5)$$

And, we take:

$$\varepsilon_0^{xx}(T) = \varepsilon_0^{zz}(T) = \varepsilon_0(T)\,, \qquad (6)$$

$$\varepsilon_0^{yy}(T) = -\varepsilon_0(T)\,, \qquad (7)$$

$$\varepsilon_0^{xy}(T) = \varepsilon_0^{yz}(T) = \varepsilon_0^{xz}(T) = 0\,. \qquad (8)$$

We assume that the shear strains in (8) are all zero since we are using Intel technology which introduces only uniaxial strains and stresses after deposition of the Si(1-x)Ge(x) thin films. The normal intrinsic strains and

stresses introduced by Intel technology for nano pMOS transistors are compressive (i.e; negative) in x and z directions and tensile (i.e positive) in y direction. These x, y, and z directions are shown in Figure 1. From equation (5), $\varepsilon_0(T)$ is negative. Then, $\varepsilon_0^{xx}(T)$, and $\varepsilon_0^{zz}(T)$ are compressive and $\varepsilon_0^{yy}(T)$ is tensile. The models we are proposing in the equations (2)-(8) to calculate the thermal mismatch induced intrinsic strain in Si(1-x)Ge(x) thin films are original, accurate, in 3D, and physically based. Now, we use the equation (1) and the equations (2)-(8) to calculate accurately all the 3D components of the thermal mismatch induced intrinsic stress $\sigma_0^{tm}(T)$ in the Si(1-x)Ge(x) thin films as follows:

$$\begin{aligned}
\sigma_0^{xx}(T) &= (c11+c12).\varepsilon_0^{xx}(T)+c12.\varepsilon_0^{yy}(T)\\
\sigma_0^{yy}(T) &= (c11+c12).\varepsilon_0^{xx}(T)+c11.\varepsilon_0^{yy}(T)\\
\sigma_0^{zz}(T) &= (c11+c12).\varepsilon_0^{zz}(T)+c12.\varepsilon_0^{yy}(T)\\
\sigma_0^{xy}(T) &= \sigma_0^{yz}(T)=\sigma_0^{xz}(T)=0
\end{aligned} \tag{9}$$

Where c11, and c12 are the elastic constants of Si(1-x)Ge(x) films. We have used Vegard's Law (Denton et al., 1991) to calculate them as follows:

$$cij=(1-x).cij(Si)+x.cij(Ge).$$

Where cij(Si), and cij(Ge) are the elastic constants of Si and Ge materials at room temperatures and i,j=1,2. The model proposed here in (9) to calculate the thermal induced intrinsic stress σ_o (= $\sigma_0^{tm}(T)$) in Si(1-x)Ge(x) films is also original, accurate, and physically based. It is original since:

Firstly, we are taking into account the effects of both the thermal expansion mismatch $\Delta\alpha(x,T)$, growth temperatures T, and Ge mole fraction x. Secondly, this model can be used to calculate separately the intrinsic stress σ_o that is due only to thermal mismatch. We should know that the intrinsic stress σ_o obtained from measurements includes both the effects of thermal mismatch and lattice mismatch and even other source of stress like doping, neighboring, layout, annealing, etching, packaging, capping layers and more. Then, we cannot use the values of σ_o coming from measurements to investigate and quantify only the effects of the thermal mismatch or only the effects of lattice mismatch. Designers, engineers, and manufacturers would like to know for example which kind of effects are dominant for improving the performances of nano pMOS: thermal mismatch effects or lattice mismatch effects. For some devices, thermal effects are dominant. For other devices, the lattice mismatch effects are dominant. Sometimes the lattice mismatch effects are dominant for a certain range of growth temperatures and the thermal mismatch effects become dominant for another range of temperature (Alireza et al., 2013). From the model in (9), we can quantify the amount of intrinsic stress σ_o that results from thermal mismatch only.

As far as we know, no theoretical model has been proposed in the published literature to calculate the initial stress σ_o in Si(1-x)Ge(x) films. To quantify the amount of intrinsic stress σ_o originating only from the lattice mismatch, we need to use another model which is not in the scope of this paper. The model in (9) is based on Hooke's law. And, it is accurate since the models we have used to calculate the temperature dependence of the TECs of Si, Ge, and Si(1-x)Ge(x) films are in excellent agreement with measurements. The justification of the model in (5) for thermal mismatch strain is based on the definition of the thermal expansion coefficient. In general, the thermal expansion $\alpha(T)$ is defined as the rate of change of the thermal strain $\varepsilon(T)$ with respect to temperature as follows:

$$\alpha(T)=\frac{d\varepsilon(T)}{dT}. \tag{10}$$

We have applied this formula to the Si(1-x)Ge(x) films when they are free and when they are attached to the substrate to get the model in (5). We should note that the thermal strain defined in a material is different from the thermal mismatch strain which is defined at the interface between two different materials. The model we proposed in (5) is for thermal mismatch strain. Now, we are going to present the models we are using to calculate the thermal mismatch induced extrinsic stress σ which is defined in the whole structure of 14 nm pMOS transistor. The extrinsic stress σ is generated from the intrinsic stress σ_o that exists in the SiGe films after their growth. To calculate σ, we use the following procedure:

a) We calculate the extrinsic stress tensor σ from the extrinsic strain tensor ε and σ_o by using Hooke's law as follows:

$$\sigma = D\varepsilon - \sigma_0 \tag{11}$$

$$\varepsilon=(\varepsilon^{xx},\varepsilon^{yy},\varepsilon^{zz},\varepsilon^{xy},\varepsilon^{yz},\varepsilon^{xz})$$

$$\sigma=(\sigma^{xx},\sigma^{yy},\sigma^{zz},\sigma^{xy},\sigma^{yz},\sigma^{xz})$$

b) We calculate the components of ε from the displacements u, v, and was described in (El Boukili, 2015).

c) We use Finite Volumes method to calculate numerically the displacements u, v, and w by solving a system of a second order partial

differential equations described in (El Boukili, 2015).

We should note that the intrinsic stress σ_0 in Equation (11) is equal to the thermal mismatch induced stress $\sigma_0^{tm}(T)$ in Si(1-x)Ge(x) films. And, we assume that σ_0 is equal to zero in all the remaining parts of the Si substrate. This is assumption is valid since the Si substrate is thick and there will be no intrinsic stress build up in it. From the proposed model in (11), we can study, analyze, and quantify the effects of the thermal expansion mismatch $\Delta\alpha(x,T)$, growth temperatures T, and Ge content x on the extrinsic stress σ. And, this will allow us to study and quantify the effects of the same parameters $\Delta\alpha(x,T)$, T, and x on the speed performances of all the modern nano pMOS transistors. The reason is that the mobility of holes increases with decreasing compressive stress σ according to (JianLi et al., 2014; Kumar et al., 2012; Moroz et al., 2013, 2012, ,2006, 2004). And, we know that the speed of nano pMOS will increase if we increase the mobility of holes. The speed of nano pMOS is related to the mobility of holes (see El Boukili, 2015) and the mobility of holes is directly related to the extrinsic stress σ (see JianLi et al., 2014; Kumar et al., 2012). And, the extrinsic stress σ is directly related to the intrinsic stress σ_0 from Equation (11). And, finally the intrinsic stress σ_0 is related to $\Delta\alpha(x,T)$, T, and x as can be seen from the proposed models (2)-(9).

5. SIMULATION RESULTS, VALIDATION, AND ANALYSIS

In this section, we are going to apply, analyze, and validate the proposed models in the Equations (1) to (11) to calculate accurately the thermal mismatch induced extrinsic stress σ in 14 nm nano pMOS transistor developed by Intel in 2014. The gate length (Lg) of this device is 23 nm. Its source and drain are made up of Si(1-x)Ge(x) thin films that are used as stressors (see Figure 1). Their thicknesses are 60 nm. Their lengths are 288.5 nm. The length in x direction of the Si substrate is 300 nm. The thickness of Si substrate in y direction is 190 nm. And, the width of the Si substrate in z direction is 300 nm. The Si substrate orientation is (100). And, the channel orientation is <110>.

5.1. Simulation results and validations

In the following Figures 2, 3, and 4 the growth temperature T is 600°C.

Figure 2 shows the 3D distribution of thermal induced extrinsic stress σ^{xx} when x=20%, $\Delta\alpha(x,T)$ = -0.7934e-6 /°C.

Figure 3 shows the 3D distribution of the thermal induced extrinsic stress σ^{xx} when x=30%, $\Delta\alpha(x,T)$ = -1.19e-6 /°C.

Figure 4 shows the 3D distribution of the thermal induced extrinsic stress σ^{xx} when x=40%, $\Delta\alpha(x,T)$ = -1.586e-6 /°C.

In the following Figures 5, and 6 the Ge content x is 20%.

Figure 5 shows the cross-section distribution of the thermal induced extrinsic stress σ^{xx} when $\Delta\alpha(x,T)$ = -0.847e-6 /°C and the fabrication temperature T=700°C.

Figure 6 shows the cross-section distribution of the thermal induced extrinsic stress σ^{xx} when $\Delta\alpha(x,T)$ = -1.007e-6 /°C and the fabrication temperature T=1000°C.

The obtained results for σ^{xx} are qualitatively in excellent agreement with the simulation and the experimental results found in literature. From Figure 2, where x=20%, and Si(80%)Ge(20%) film is the only stressor, σ^{xx} = -1.117e+8 Pa at the center of the channel. And, σ^{xx} = -3.0034e+7 Pa just below the center of the channel. The simulation results found in (Moroz et al., 2005) for a pMOS structure with Si(80%)Ge(20%) films in source and drain are: σ^{xx} =-10e+8 Pa at the center of the channel, and, σ^{xx} =-5e+8 Pa just below the channel. The shape of σ^{xx} in Figure 2 is very close to shape of σ^{xx} in (Moroz et al., 2005). So, our simulation results are qualitatively in good agreement with those of (Moroz et al., 2005). We believe that our values are smaller than those of (Moroz et al., 2005) since in our simulations we are using only one stressor (Si(1-x)Ge(x)) and our σ^{xx} is due to thermal mismatch only. The σ^{xx} in (Moroz et al., 2005) is bigger since it represents the sum of the compressive stresses coming from: thermal mismatch, lattice mismatch, layout effects, and capping layer.
Our simulation results are, also, qualitatively in good agreement with the simulation results found in (Alireza et al. 2013; Moroz et al., 2012, 2006). They are also in good agreement with measurements found in (Peng et al., 2006; Heicker et al., 2007).

5.2. Discussion and analysis

From Figures 3, 4, and 5, we can see that the compressive stress σ^{xx} is decreasing with increasing Ge mole fractions and the thermal expansion mismatch $\Delta\alpha(x,T)$ when the fabrication temperature T is 600°C. According to the Figure 7 from (Packan et al., 2008), the hole mobility is increasing with decreasing compressive stress σ^{xx}. And, the speed of nano pMOS transistors is increasing with increasing hole mobility. We could, then, conclude that the hole mobility and the speed of 14 nano pMOS will increase with increasing Ge content x and with increasing thermal expansion $\Delta\alpha(x,T)$. On the other hand, we already know that the hole mobility increases with increasing Ge content x for 35 nm or above technology node of pMOS (Moroz et al., 2006). However, and as far as we know, no investigation has been done about the effects of Ge content x for 14 nm technology node for pMOS.

The most important achievement and the originality of this paper is the calculation of the amount of stress σ^{xx} that is due to solely thermal mismatch effects. From Figure 4 the amount stress σ^{xx} at the center of the channel that is due to the thermal mismatch $\Delta\alpha(x,T)$ =-1.586e-6/°C for x=40% and T=600°C is -1.8028e+8 Pa. And, from the Figure 7, we could see the effects of this amount of thermal stress on the hole mobility enhancement. In published simulation results (Moroz et al., 2013, 2012, ,2006, 2004; Peng et al., 2006), the calculated values of σ^{xx} involve so many effects: thermal mismatch effects, lattice mismatch effects, layout effects, doping effects, capping layers effects, and more. Therefore, from published results, we cannot quantify the contribution of solely thermal mismatch effects on the hole mobility and speed performance of nano pMOS transistors.

Another originality of this paper is the calculation of the amount of thermal stress σ^{xx} for different thermal expansion mismatch $\Delta\alpha(x,T)$ between Silicon substrate and Si(1-x)Ge(x) films and different temperatures T. In practice, when we change x is like we have a different material. So, different values of x give us different materials with different mechanical properties. This analysis is then beneficial for Concentrators Photo Voltaic (CPV) Solar Cells with multi-junctions or even for Silicon based single junction solar cells working in arid regions where the temperature is high like the desert of Morocco or elsewhere. The high operating temperatures (sometimes above 100°C) cause thermal expansions of the materials making up the solar cell which may generate high thermal strains and stresses and which may reduce the efficiency by 50% or more.

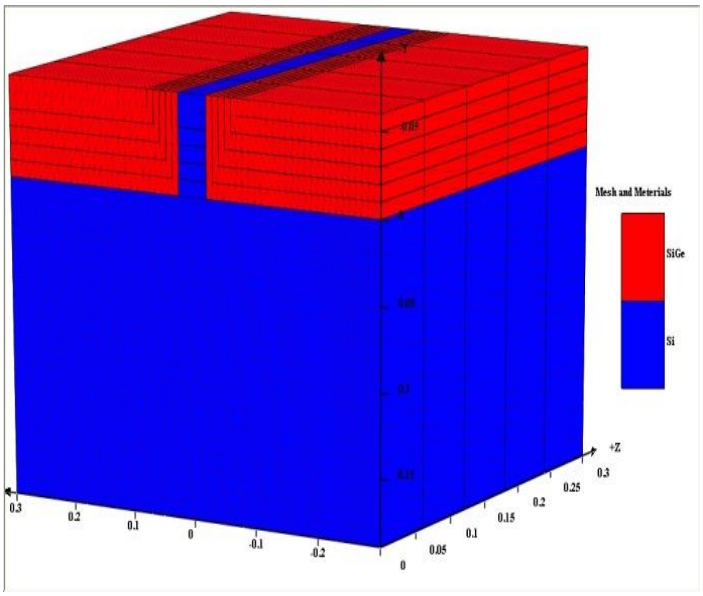

Figure 1: Materials And Mesh Of The Simulated Structure: 14 nm nano pMOS Transistor.

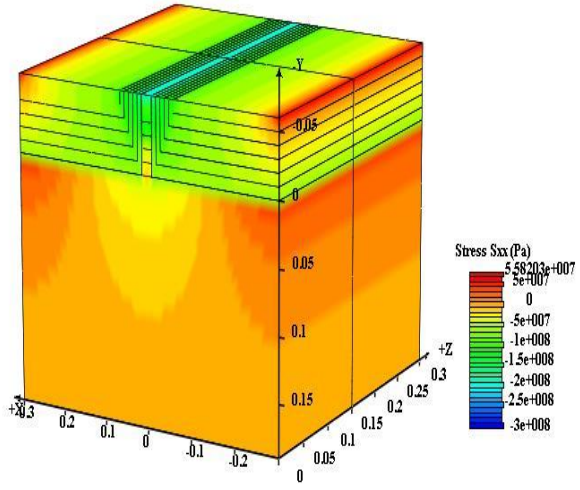

Figure 2: 3D Distribution of σ^{xx} When x=20%, $\Delta\alpha(x,T)$ = -0.7934e-6/°C, And T=600°C.

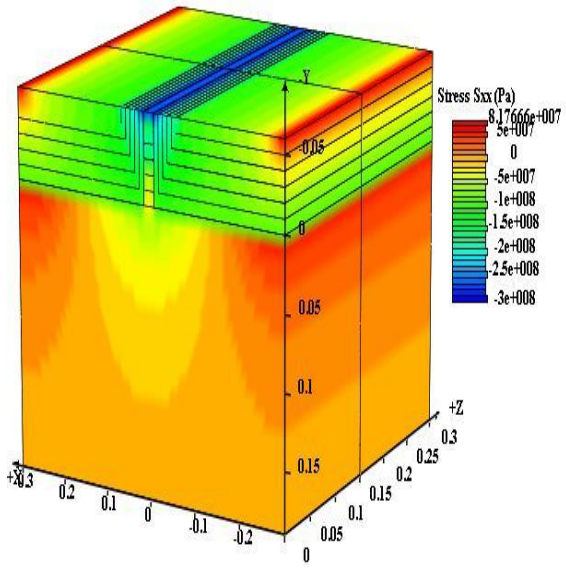

Figure 3: σ^{xx} When x=30%, $\Delta\alpha(x,T)$ = -1.19e-6 /°C, And T=600°C.

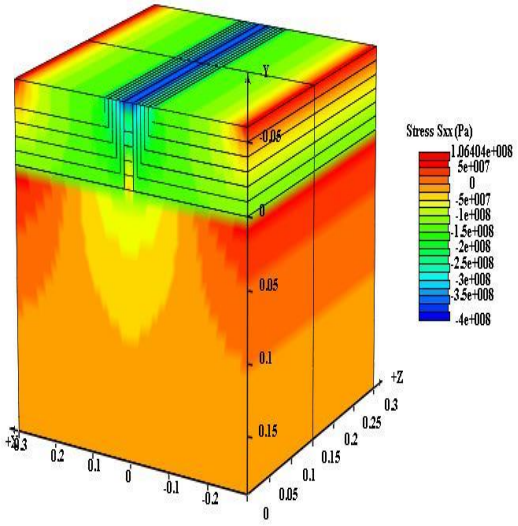

Figure 4: σ^{xx} When x=40%, $\Delta\alpha(x,T)$ = -1.586e-6 /°C, And T=600°C.

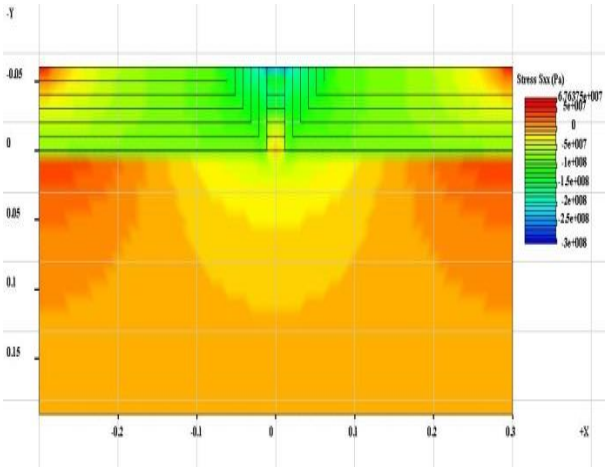

Figure 5: σ^{xx} When x=20%, $\Delta\alpha(x,T)$ =-0.847e-6 /°C , And T=700°C.

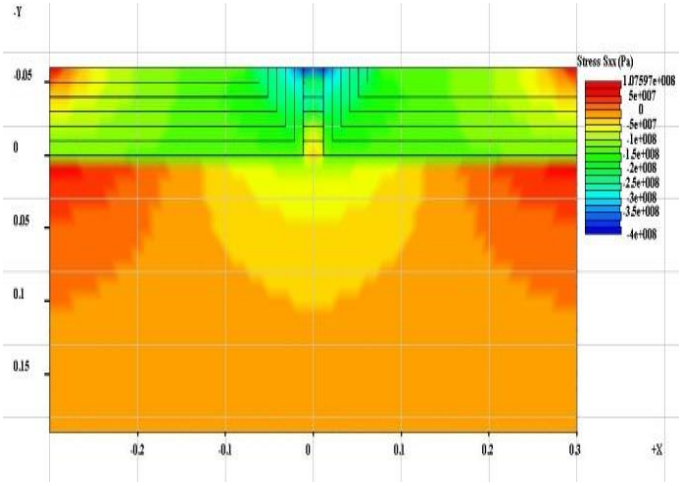

Figure 6: σ^{xx} When x=20%, $\Delta\alpha(x,T)$ = -1.007e-6/°C, And T=1000°C.

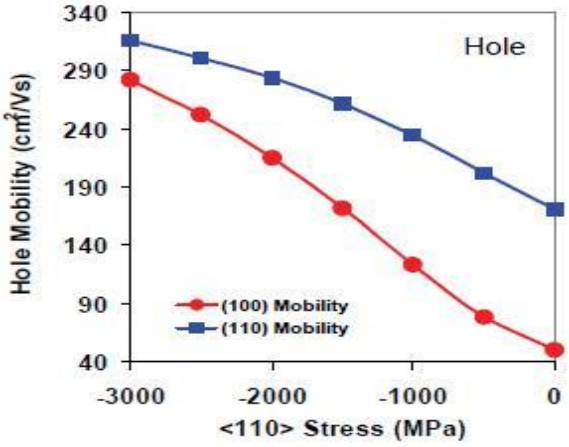

Figure 7: Compressive Stress (σ^{xx}) Enhanced Hole Mobility From (Packan et al., 2008).

6. CONCLUSIONS

In this paper, we have developed, validated, and applied original, accurate and physically based models to simulate and analyze the effects of solely thermal expansion mismatch between Silicon substrate and Si(1-x)Ge(x) films on the speed performance of 14 nm nano pMOS transistors developed by Intel in 2014. Our numerical results in Figures 2, 3, and 4 show that the amount of thermal stress obtained for different thermal expansion mismatch for x=20%, 30%, and 40% is between -1.8028e+8 Pa and -1.117e+8 Pa. This is a great finding for engineers, designers, and manufacturers. Since it shows the effects of thermal mismatch induced stress on the speed performance of 14 nm nano pMOS transistors. In the future, we will investigate the effects of both thermal mismatch and lattice mismatch of the hole mobility and the speed performances of nano pMOS devices.

REFERENCES

Alireza, M., Haihui, R., Zhang, L., Mei, L.,(2013). Residual stresses in thin film systems: effects of lattice mismatch, thermal mismatch and interface disloactions. Int. Jour. Of Solids, Vol. 50, 3562-3569.

Bera, L.K., 2006. The impact of uniform strain applied via bonding onto plastic substrate on MOSFET performance. IEEE Electron Device Lett., Vol. 27, 58-61.

Chui, K.J., 2007. n-MOSFET with silicon-carbon source/drain for enhancement of carrier transport. IEEE Trans. Electron Devices, Vol. 54, 249-256.

Denton, A. R.; Ashcroft, N. W. (1991). Vegard's law. Phys. Rev., A 43 (6), 3161–3164.

El Boukili, A., 2010. 3D Stress simulations of nano transistors. In: Gunther, M., Bartel, A., Brunk, M., Schops, S., Striebel, M., eds. Progress in Industrial Mathematics at ECMI. Berlin Heildelberg: Springer, 85-91.

El Boukili, A., 2015. New models for thermal stress simulation in 3D nano CMOS transistors. Proceedings of the first international conference on electrical and information technologies. pp. 25-27, March, 25-27, Marrakech (Morocco).

Ghani, T. et al., 2003. A 90nm high volume manufacturing logic technology featuring novel 45nm gate length strained silicon CMOS transistors. Proceedings of IEDM Technical Digest, pp.978-980. Dec. 8-10, Washington DC (USA).

Ghani, T., 2010. Challenges and innovations in nano-CMOS transistor scaling. IEEE workshop on microelectronics and electron device. April 16, Boise (Idaho USA).

Hecker, M., Geisler, H., (2007). Strain state in silicon structures for microprocessors technology. Materials Science-Poland, Vol. 25, No. 1, 7-18.

JianLi, M., Fu, Z., Liu, P., Zhang, H. (2014). Hole mobility enhancement in uniaxial stressed Ge dependence on stress and transport direction. Science China, Phys., Mech. & Astr., Vol. 57, 1860-1865.

Kumar, A., Xiu, K., Haensch, W., Robinson, R., Bajaj, M., Johnson, J., Furkay, S., Williams, R. (2012). A simple, unified 3D stress model for device design in stress-enhanced mobility technologies. Proceedings of SISPAD, pp. 3000-3003, Sept. 5-7, Denver (CO, USA).

Moroz, V., 2004. Analyzing strained-silicon options for stress-engineering transistors. Solid State Technology Magazine. July, Vol. 47, issue 7, p49.

Moroz, V., Eneman, G., Nouri, F., Smith, L., (2005). The impact of layout on stress-enhanced transistor performance. Proceedings of Int. Conf. on Simulation of Semiconductor Processes and Devices, pp. 143-146. Sept. 1-3, Tokyo (Japan).

Moroz, V., Washington, L, Farah, N., Sunderraj, T., Eneman, G., Smith, L., Screntelkamp, R., (2006). pMOS with 200% mobility enhancement induced by multiple stressors. IEEE Electron Dveice Letter, Vol. 27, No. 6, 511-513

Moroz, V., et al., 2012. 14nm FinFET stress engineering with epitaxial SiGe source/drain. Proceeding of ISTDM, pp. 1-2. June 4-6, Berkeley (CA, USA).

Moroz, V., et al., 2013. A group IV solution for 7nm FinFET CMOS: Stress engineering using Si,Ge, and Sn. Proceeding of IEDM, pp. 26.3.1-26.3.4 Dec. 9-11, Washington DC (USA).

Okaji, M., Yamada, N., Watanabe, H., (2004). Linear thermal expansion of Silicon from 293 to 1000 K. International Journal of Thermodynamics, Vol. 25, No 1, 221-236.

Okada, Y., Tokumaro, Y., Watanabe, H., (1984). Precise determination of lattice parameter and thermal expansion coefficient of Silicon between 300 and 1500°K. Journal of Applied Phys., Vol. 56, No 2, 314-320.

Packan, P., Cea, S., Desphande, H., Ghani, T., Giles, M., Panale, P., Zawadzki, K., (2008). High performance high-K+ metal gate strain enhanced transistors on (110) silicon. *Proceedings of IEDM*, pp. 1-4, Dec. 15-17, San Francisco (CA,USA).

Peng, Z., Andrei, A., Haifeng, H., Joel, W., Chris, N., Eric, S., (2006). Analysis of nano-scale stress in strained silicon materials and microelectronics devices by energy-filtered convergent beam electron diffraction. ECS Transactions, 2(2), 559-568.

Singh, H., (1968). Determination of thermal expansion of Germanium, Rhodium, and Iridium by X-rays. Acta Cryst., Vol. A 24, No 2, 469-471.

Yin, Z., Zhu, J., He, Q., Cao, X., Tan, C., Chen, H., (2006). Graphene-based materials for solar cell applications. Advance Energy Materials, Vol. 4, No. 1, 1-19.