SIMULATION AND MODELLING OF THE FLAT-BAND VOLTAGE FOR BELOW 200nm SOI DEVICES

C. Ravariu[1], F. Babarada[1]
[1] Politehnica University of Bucharest, Faculty of Electronics and Telecommunications, Splaiul Independentei 313, 060042, Bucharest, Romania,
E-mail: cristir@mcma.pub.ro
and babflorin@yahoo.com

ABSTRACT
The nowadays SOI technologies frequently offer below 200nm, even up to tens of nanometre, for film on insulator. The flat-band voltage is one of main parameter in the electrical characterization of the SOI devices. The conventional models for this voltage were established for thicker structures, with 0.5...2μm Si-film thickness and 2-3μm buried oxide thickness. The electric charge from the buried oxide was ignored because the interesting conduction occurs in the vicinity with the front oxide.
The pseudo-MOS transistor is a dedicated device for the electrical characterization of SOI wafers and works with a buried channel. The downscaling consequences of the SOI sizes on the flat-band voltage modelling were studied in this paper, with applications on the pseudo-MOS device.

KEY WORDS
Modelling, simulation, SOI, buried interface, devices

1. Introduction

The algorithm of modelling and simulations of physical processes spread over a large spectrum of applications, [1], [2]. The SOI structures represent a promising candidate for the nanodevice implementation, as classical [3] or novel architecture, [4]. This miniaturization is possible only if it is accompanied by proper models for the developed electronics devices. Some device parameters lost or change their classical meaning for new technologies. For example, the threshold voltage cannot be defined in a SON Transistor, [5], but it still arises in the transfer characteristics of a pseudo-MOS device, [6].

An excellent device for the electrical characterization of the SOI wafers is the pseudo-MOS transistor. This device represents an up-side-down SOI-MOSFET, with a back-gate command and electrical conduction through the film bottom, [7]. This paper comparatively presents some new analytical models, versus some simulation results, regarding the flat-band voltage of a pseudo-MOS transistor.

A new reference model will be confronted with others, analytically deduced in the next paragraph. A comparative analysis between the classical model, new model and the simulation results are presented, as novelty.

2. The analytical model

The definition of the flat band voltage is related to the compensation of the positive electric charges from the buried insulator in order to bring the film surface potential to zero volts.
Adapted from the SOI-MOSFET to the pseudo-MOS transistor, this parameter is classically expressed as, [8]:

$$V_{FB} = -\frac{Q_{it}}{2C_s} - \frac{Q_{it}^2}{2q\varepsilon_{Si}N_A} + \Phi_{MS} \qquad (1)$$

where N_A [cm^{-3}] is the doping concentration in substrate, Qit [e/cm^2] is the surface electric charge density, Φ_{MS} [V] is the metal-semiconductor work function, $C_s=\varepsilon_{ox}/x_{ox}$ [F/cm^2] is the specific oxide capacitance, $\varepsilon_{Si/\ ox}$ is the dielectric permittivity of Silicon, respectively oxide, x_{ox} is the BOX (Buried Oxide) thickness and $q=1{,}6x10^{-19}C$ is the elementary electric charge. Firstly, in the analytical model Φ_{MS} =0V will be assumed.

At the interface Si/SiO_2 usually exists a positive electric charge, Q_{it}, due to the presence of two kinds of charges: the interface charge Q_t representing the electrons trapped on the fast surface states and the fixed charge Q_f representing an excess of the ionic silicon solved in oxide and frozen at the Si/SiO_2 interface during the end of the annealing. The global charge is noted in this paper by $Q_{it} = Q_t + Q_f$.
Its sub-components can be: $Q_{t1}=10^9 \div 10^{10} e/cm^2$, $Q_{t2}=10^{10} \div 10^{11} e\ /cm^2$, $Q_{f1}=10^{10} e/cm^2$, $Q_{f2}=10^{12} e/cm^2=10^{-2} e/nm^2$; where the index "1" is used for the upper SOI interface and "2" for the bottom SOI interface. Frequently, the effect of Q_t on V_{FB} is neglected. For example, the contribution of Q_t charge is just 0,01V in V_{FB} value for the density of states $10^{10} eV^{-1}cm^{-2}$ in a bulk MOSFET with $N_A=10^{15}cm^{-3}$ and x_{ox}=100nm.

Therefore, in this paper we will work with the total positive electric charge Q_{it1}, Q_{it2} were considered, fig. 1. The flat-band voltage represents that gate voltage, which reduce to zero volts the potential in the Si-film, equivalent

with V(0)=0 and E(0)=0 in fig.1. By integration of the Poisson's equation, yields:

$$V_{FB} = \left(-\frac{Q_{it1}}{C_s} \right) + \left(\frac{qN_A}{2\varepsilon_{Si}} x_d^2 - \frac{Q_{ox1} + Q_{ox2}}{\varepsilon_{Si}} x_d \right) \qquad (2)$$

The first parenthesis represents the potential drop over the buried oxide and the second parenthesis is the potential drop over substrate. The notations correspond to the fig. 1, where x_d is the width of the depleted region in substrate.

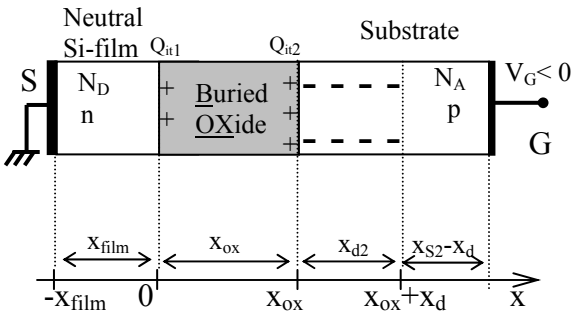


Fig. 1. The analyzed SOI structure with positive fixed charges in BOX and negative ions in substrate.

The limit conditions give the electric field:

$$\varepsilon_{ox} E_{ox}(0) - \varepsilon_{Si} E_{Si}(0) = Q_{it1} \Rightarrow E_{ox} = \frac{Q_{it1}}{\varepsilon_{ox}} \qquad (3)$$

$$\varepsilon_{Si} E_{SB}(x_{ox}) - \varepsilon_{ox} E_{ox}(x_{ox}) = Q_{it2} \Rightarrow$$
$$E_{SB}(x_{ox}) = \frac{Q_{it1} + Q_{it2}}{\varepsilon_{Si}} \qquad (4)$$

From Gauss'law for $x \in (x_{ox}, x_{ox} + x_d)$ results:

$$E_{SB}(x) = -\frac{qN_A}{\varepsilon_{Si}} \cdot (x - x_{ox}) + \frac{Q_{it1} + Q_{it2}}{\varepsilon_{Si}} \qquad (5)$$

From the limit conditions: $E_{SB}(x_{ox}+x_d)=0$ in (5), the x_d expression results:

$$x_d = \frac{Q_{it1} + Q_{it2}}{qN_A} \qquad (6)$$

By replacing x_d from (6) in (2), the final expression of V_{FB} is obtained:

$$V_{FB} = -\frac{Q_{f1}}{C_s} - \frac{(Q_{it1} + Q_{it2})^2}{2\varepsilon_{Si} qN_A} \qquad (7)$$

The traditional Lim and Fossum model completely ignores the second interface, considering $Qit_2=0$ and also the depletion of the substrate, $x_{d2}=0$, [6]. Hence, V_{FB} is $-Q_{it1}/C_s$. This happened at the beginning of the SOI structures, with Micronics sizes. Obviously, "Q_{it}" is a model parameter in (1) and hasn't a physical meaning. It is named "the global charge from BOX", but from eq. (1) it must be measured in [C/cm^2], being a superficial electrical charge density.

A first disagreement between models (1) and (7) consists in different values of Q_{it}, and $Q_{it1}+Q_{it2}$. Considering additionally the electric charge from the second interface $Qit_2 \neq 0$, from the limit conditions the accurate model is (7). The classical model (1) systematically under-evaluates the flat-band voltage value. Additionally, Q_{it} from the first and second ratio in eq. (1) hasn't quite the same values.

Another correction concerns the "2" factor that is missing in the model (7), first fraction at denominator, due to an average value assigned to Q_{it}.

In fact, either interface comprises fixed charges Q_f and interface trapped charges, Q_t. Consequently, the model (7) can be detailed as:

$$V_{FB} = -\frac{Q_{f1} + Q_{t1}}{C_s} - \frac{(Q_{f1} + Q_{t1} + Q_{f2} + Q_{t2})^2}{2\varepsilon_{Si} qN_A} \qquad (8)$$

where $Q_{t1,\,2}$ respectively are the electric charge densities due to the electrons captured on the fast-states from the Si-film/BOX and BOX/Substrate interfaces. The correct value of the fixed charge density, $Q_{f\,1,\,2}$ must be extracted from V_{FB} parameter after the $Q_{t1,\,2}$ subtractions from V_{FB} in eq. (8). In the spirit of the classical model (1), model (8) could be corrected by averaging:

$$V_{FB} = -\frac{Q_{it1}/2}{C_s} - \frac{((Q_{it1} + Q_{it2})/2)^2}{2q\varepsilon_{Si} N_A} \qquad (9)$$

In this way, two targets are reached: the problem of "2" missing at denominator of first ratio of model (7) is solved and a better agreement between simulations and the analytical model is obtained; the second ratio from model (7) overestimate the flat-band voltage, while the second ratio from model (9) brings the analytical values closer to the simulation results. The insight for Q_{it1} must be $Q_{f1}+Q_{t1}$ and for Q_{it2} must be $Q_{f2}+Q_{t2}$.

In the following simulations, a reverse way was investigated: the interface global charge densities were selected for different pseudo-MOS transistors and the flat-band voltage was extracted from definition. The scope was to accomplish the best fitting between $V_{FB\ simulated}$ and $V_{FB\ analytical}$.

3. Simulations

The simulated SOI structure had: $\Phi_{MS1}=\Phi_{SM2}=-0,32V$, as is shown in fig. 2, $\Phi_{s-s}=0$, selecting the same p-type semiconductor as film and substrate with $N_A=5x10^{15}cm^{-3}$.

The interface charge densities were chosen accordingly with some typical experimental results, [9]. The total front charge $Q_{it1}=5\times10^{10}e/cm^2$ placed at x=0 in fig.1 and the total bottom charge, $Q_{it2}=5x10^{11}e/cm^2$ placed at $x=x_{ox}$ in fig.1, was selected. None charge in the front oxide was select, in order to be focused just on the buried oxide.

The simulations started with an SOI structure having x_{film}=200nm and continue to 50nm, x_{ox}=400nm, x_{SB}=750nm. Figure 2 presents the simulation results for a pseudo-MOS with 200nm. In these conditions, a holes distribution still arises along the structure.

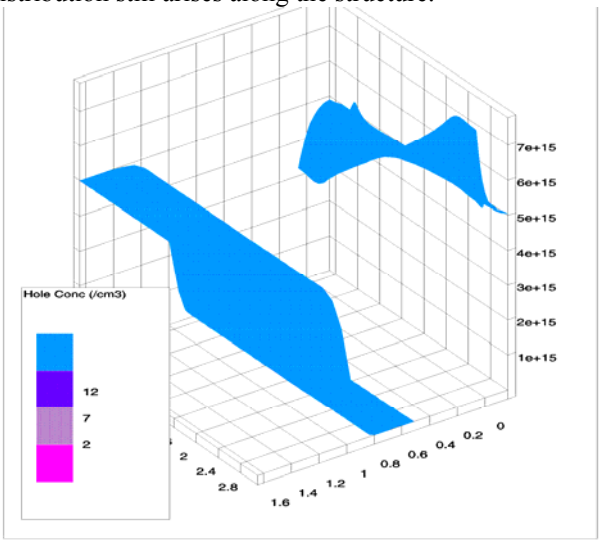
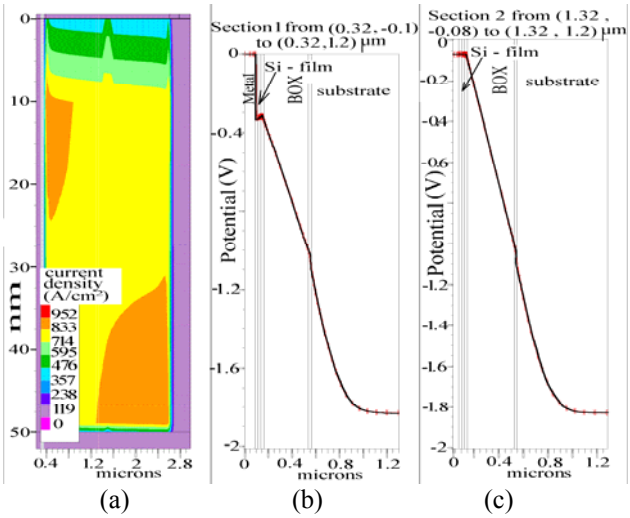


Fig.2. The holes concentration in 200nm Si-film structure.



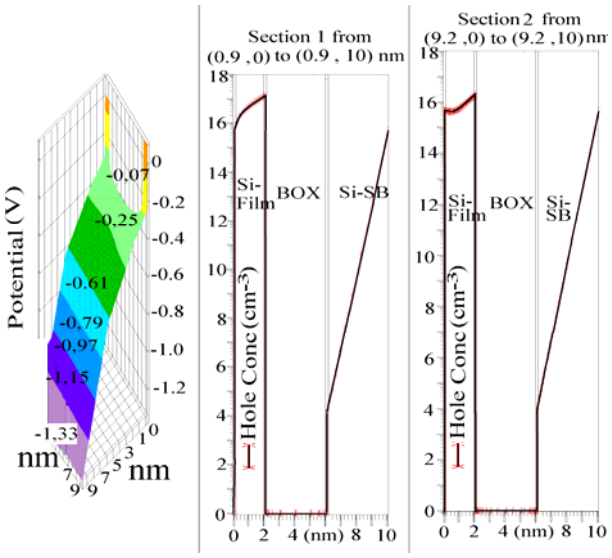
(a) (b) (c)

Fig. 3. (a) Detail of the current density in the 50nm SOI Si-film biased at V_S=0V, V_D=0,5V, V_G=-1,5V; (b) the potential distribution across the SOI near the source contact; (c) the potential distribution across the SOI through the middle.

In this case a global values $Q_{it1,\ 2}$ values were established, as is modelled in (9).

Therefore, the discussion regarding the subtracting of the $Q_{t1,\ 2}$ from the global density $Q_{it\ 1,\ 2}$ resting just at theoretical level. However the simulation can reveal some discrepancies between the classical model (1) and the proposed models (7) and (9).

Figure 3 a presents the current flow density through the Si-film in the case of biased structure at: V_S=0V, V_D=0,5V, V_G=-1,5V. The conduction prevails through the film bottom as is expected. Figures 3,b and c provide the adopted method for the extraction of the simulated flat-band voltage, V_{FBsim}. The gate voltage was increased in modulus till the film potential becomes zero. Then, the potential graph was translated with -0.32V value, correcting the metal-semiconductor work function, in order to extract the simulated flat-band voltage, $V_{FBsim=}$-1.92V, affected just by the surface electric charges densities, $Q_{ox1,\ 2}$.



(a) (b) (c)

Fig.4. The 2nm Si-film structure at V_S=0V, V_D=0.5V, V_G=-1.33V: (a) potential distribution, (b) holes concentration near source, (c) holes concentration near drain.

Accordingly with fig. 4.a, at V_G=-1,33V applied on the back gate, the hole concentration $p>10^{16}cm^{-3}>N_A$. Hence a lower flat-band voltage is searching.
Finally, $V_{FB\ sim}$ =-0.85V for previously mentioned $Q_{it1,\ 2}$ values.

6. Discussions

For the investigated SOI structures, with x_{film}=50nm, x_{ox}=400nmnd SOI with x_{film}=2nm, x_{ox}=4nm, the same amount of positive interface charge density was used for both structures in order to provide a comparison. These

contributions were centralized in the table 1. Here can be compared some situations simulated and computed for different sizes. The notations are: $V_{FB\ sim}$ for the simulated value of V_{FB}, $V_{FB(1)}$ for the value deduced with the model (1), $V_{FB(7)}$ for the value deduced with the model (7), $V_{FB(11)}$ for the value deduced with the model (9).

x_{film} (nm)	x_{ox} (nm)	Q_{it1} (ecm^{-2})	Q_{it2} (ecm^{-2})	$V_{FB(1)}$ (V)	$V_{FB(7)}$ (V)	$V_{FB(11)}$ (V)	V_{FBsim} (V)
50	400	$2\cdot10^{10}$	$5\cdot10^{11}$	-0.191	-4.51	-1.31	-1.82
50	400	$5\cdot10^{10}$	$5\cdot10^{11}$	-0.501	-5.55	-1.84	-1.95
50	400	$2\cdot10^{10}$	10^{12}	-0.191	-16.3	-4.32	-3.92
2	4	$2\cdot10^{10}$	10^{12}	-0.007	-15.9	-4.14	-1.95
2	4	$5\cdot10^{10}$	10^{12}	-0.042	-16.9	-4.63	-2.11
2	4	$1\cdot10^{10}$	10^{11}	-0.002	-0.18	-0.056	-0.01

Table 1: Comparisons for structures with 50nm and 2nm film thickness.

Table 1 highlight that the analytical model (1) always underestimate the flat-band voltage, considering all the time just the first interface charge, Q_{it1}. The inclusion of the second interface charge Q_{it2}, with some correct limit conditions but in the depletion approximation, systematically overestimate the flat-band voltage accordingly the model (7). The best model at thick or thin sizes is the analytical model (9).
For thinner SOI films, a lower interface area results, within a lower quantity of negative ionic charge in substrate, in order to fulfill the flat-band conditions. In the ultra-thin SOI structures, the substrate isn't inverted, being in incipient depletion regime. Hence, the depletion approximation used in the deduction of the model (7), is more justified in ultra-thin SOI films than in thicker films.
In SOI nanofilms the components Q_{f1}, Q_{f2} change the balance of importance on V_{FB} parameter. In thick BOX, some values like $Q_{it1}=10^{10}e/cm^2$, $Q_{it2}=10^{12}e/cm^2$, influence the potential of Si-film mainly via Q_{it1} parameter. In the case of some nanometres thickness of film and BOX and a device area=10x10nm^2 the prior charges densities are: $Q_{it1}=10^{12}e/cm^2$=0.01electrons/ device area – in probability terms quite negligible and $Q_{it2}=10^{12}e/cm^2$=1electron/ device area – has a strong activity through a 2-5 nm thickness of buried oxide.

6. Conclusion

The classical model (1) induces high errors in thin SOI films because it entirely ignores the back charge interface that was true at thick BOX. The model (7) accurately deduced by Poisson equation integration systematically overestimated the flat-band voltage, because it use the depletion approximation in substrate and ignore the inversion layer arisen at the substrate surface. Simulator that proved accumulation of electrons at the substrate surface surprises the superposition. Therefore, the best model is (9), based on the averaging of the known interface charge, Q_{it1} and Q_{it2}.

In conclusion the charge placed at the bottom interface BOX/Substrate has a maximum influence on V_{FB} parameter extraction in the thin SOI films and it is partially annihilated by the negative inversion layer formed at the substrate surface during the device operating, in thicker SOI films.

Acknowledgment. This work is supported by the POSDRU /89/1.5/S/**62557**, PN2 no. **12095, 62063**.

References

[1] Antonio Cimino, Francesco Longo, Giovanni Mirabelli, *A General Simulation Framework for Supply Chain Modeling: State of the Art and Case Study*, International Journal of Computer Science Issues, Volume 7, Issue 2, No 3, pp 1-9, March 2010.
[2] Michael Affenzeller, Stefan Wagner, Stephan M. Winkler, *Effective allele preservation by offspring selection: an empirical study for the TSP*, International Journal of Simulation and Process Modelling 2010 - Vol. 6, No.1 pp. 29 - 39.
[3] F. Babarada, et al., MOSFET *Modelling Including Second Order Effects for Distortion Analysis*, IASTED Proc., Applied Simulation and Modelling 2006, Rhodes, Greece, pp. 506-510.
[4] C. Ravariu, ey al., *Modelling and simulation of a nanostructure for a single electron technology implementation*, 5th International Mediterranean Modelling Multiconference, EMSS, Briatico, Italy, 16-19 Sept, 2008, ISBN 978-88-903724-0-7, pp.312-315.
[5] J. Pretet, S. Monfray, S. Cristoloveanu and T. Skotnicki. Silicon-On-Nothing MOSFETs: performance, short channels effects and back gate coupling. IEEE Trans. Electron Devices, vol.51, no.2, pp. 240-245, 2004.
[6] C. Ravariu, A. Rusu, *Parameters extraction from some experimental static characteristics of a pseudo-MOS transistor*, Bucharest, UPB Scientific Bulletin, ISSN 1454-234X, Series C, vol. 70, no. 1, pp. 29-34, 2008.
[7] S. Sato, K. Komiya, N. Bresson, Y. Omura, S. Cristoloveanu, Possible influence of the Schottky contacts on the characteristics of ultrathin SOI pseudo-MOS transistors, IEEE Transactions on Electron Devices, vol 52, no.8, pp. 1807-1808, 2005.
[8] H.K.Lim, J.G.Fossum, Threshold voltage of thin-film silicon-on-insulator (SOI) MOSFET's, *IEEE Trans. Electron. Devices,* vol. ed-30, no.10, October, 1993.
[9] CEA-Leti R&D, 20nm Fully Depleted SOI process, EUROSOI, Newsletter, October, vol XXVI, 2010.