INVESTIGATION OF THERMAL EFFECTS ON ELASTIC CONSTANTS TO SIMULATE CORRECTLY THE THERMAL STRESS IN NANO TRANSISTORS

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ABSTRACT

Mechanical stress is the main performance booster for the new generation of nano CMOS transistors. Then, accurate models to calculate this stress are requested.

In this paper, we are proposing new and accurate mathematical model to calculate numerically and correctly the thermal induced stress in the new generation of Intel nano PMOSFETs. In this model, we are taking into account, for the first time, the effects of the fabrication temperature on the elastic constants of Silicon and Silicon Germanium materials to calculate the thermal stress. Numerical results from different simulations with different temperatures for thermal induced stress in 14 nm Intel nano PMOS of the year 2014 will be given, discussed, and compared with literature.

Keywords: temperature effects, elastic constants, thermal induced stress , 3D modeling and simulation, Intel nano CMOS transistors

1. INTRODUCTION

For the last decade, mechanical stress is extensively used by many manufacturers as IBM, Intel, AMD, Toshiba, Samsung, and Infineon to increase dramatically the performance of the new generation of nano CMOS transistors (Ghani 2010, Chui 2007, JianLi 2014). It is now admitted by the semiconductor community that the application of mechanical stress to the channel enhances the mobility of both nano NMOS and PMOS transistors by more than 50% (JianLi 2014, Ghani 2010, Chui 2007, Bera 2006, Krivokapic 2003). From physics point of view, this enhancement of the mobility is due fundamentally to the splitting of the conduction and valence energy bands by the mechanical stress (Ghani 2003, JianLi 2014). And, this splitting of the energy bands results in the reduction of band gap energy. When the band gap is reduced, the mobility will be increased. The performance of CMOS transistors have been continuously improved by the traditional geometric scaling of its critical dimensions. The top traditional scaling enablers are: gate oxide thickness scaling, junction scaling, and common collector voltage scaling. The year 2000 marked the end of this CMOS traditional scaling era that lasts about 40 years. In the year 2000, the CMOS research team at Intel company have faced serious challenges when they have used the traditional geometric scaling to fabricate 90nm CMOS technology node (Ghani 2010). The top challenges for this 90nm CMOS were: the parasitic resistance, the gate leakage, and the mobility degradation due to channel ionized impurity scattering (Ghani 2010). In the beginning of 2000, Intel was the first company to introduce great innovations to overcome the traditional scaling barriers. The first innovation is the application of uniaxial process induced stress to enhance dramatically the channel mobility of 90nm CMOS node and below. The second innovation introduced in 2008 for 45nm CMOS node (45nm SRAM and 45nm CPU) is the use of mechanical stress and the use of high dielectric constant materials for gate insulation to help address gate leakage, and the metal gate to replace poly-silicon. In its innovations, Intel has used a Silicon Nitride capping layer to enhance the mobility of nano NMOS transistors by more than 30% (Ghani 2010). For nano PMOS transistors, Intel has used compressed Silicon Germanium (Si(1-x)Ge(x)) pockets in source and drain to introduce intentionally a compressive uniaxial extrinsic stress σ in the channel. Here x represents the germanium mole fraction. The compressive stress σ enhances the mobility of holes by more than 50% (JianLi 2014, Chui 2007, Ghani 2003). According to the predictions in (Ghani 2010), the application of this compressive stress will continue enhancing the mobility of the future nano PMOS of 16nm node, in 2016, and beyond.

The extrinsic stress σ is due to an initial (or intrinsic) stress σ_0 that builds in Si(1-x)Ge(x) pockets after high temperature epitaxial deposition of these Si(1-x)Ge(x) pockets on top of Silicon substrate. Physically, this intentional initial stress σ_0 is due mainly to material mismatch and thermal mismatch. In this work, we are focusing on how to calculate accurately the intrinsic stress σ_0 and the resulting extrinsic stress σ that are due to thermal mismatch. The thermal mismatch stress is due to the mismatch between the thermal expansion

coefficients of Silicon substrate, $\alpha_{Si}(T)$, and Si(1-x)Ge(x) pockets, $\alpha_{SiGe}(T)$. Here, T represents the deposition temperature.

In this paper, three things are new: (1) The development of new and accurate models to include the effects of the fabrication temperature on elastic constants C11 and C12 of Silicon, Germanium, and Silicon Germanium materials. (2) We use, for the first time, these temperature dependent elastic constants to calculate the thermal induced initial stress σ_0 in Si(1-x)Ge(x) thin films. (3) We use this thermal induced initial stress σ_0 to calculate numerically the resulting extrinsic stress σ in the whole structure of 14nm PMOS transistor based on Intel technology.

In our previous work (El Boukili 2015), we have proposed and used the following model to calculate the thermal induced initial tress σ_0 in Si(1-x)Ge(x) thin films after deposition:

$$\sigma_0 = D.\varepsilon_0(T) \quad (1)$$

where $\varepsilon_0(T)$ represents the initial strain tensor due to temperature. And, D represents the stiffness tensor of the elastic constants C11, C12, and C44. The definition of D will be given in Section 3. In our previous model (El Boukili 2015), D was independent of temperature. It was calculated at room temperature T0. In this paper, we are proposing a new model that includes the effects of temperature on elastic tensor D. Then, the stiffness tensor D in Equation (1) will be replaced by D(T). And, the model in Equation (1), will be replaced by the new model given in Equation (2). The model in Equation (2) does improve and enhance considerably the model in Equation (1) since it does include the effects of temperature on the elastic constants. And, this is what makes this paper relevant for the semiconductor community. As far as we know, no one has used the model in Equation (2) in literature. The use of this new model allows correct calculation of the thermal induced stress in the channel of nano PMOS transistors. And, this thermal stress is used by manufacturers as Intel to enhance dramatically the electrical and optical performances of the new generation of nano PMOS and NMOS transistors (Ghani 2010). And, this will have a great impact on economy and social life. Nanotransistors are currently the backbone for today's economy. Intel estimates about 10 million nanotransistors are shipped every year. The knowledge of the physics of transistors at the nonometer scale is, however, only theoretical. So, the understanding of the physical behavior of the nanotransistors can only happed via theoretical models and computer simulations which is the main objective of this paper.

This paper is organized as follows. Section 2 will outline the main sources of intrinsic stress in Si(1-x)Ge(x) films after high temperature deposition. Section 3 will present the new models for temperature dependent elastic constants of Silicon substrate and Si(1-x)Ge(x) thin films. It will also present the mathematical models we are using to calculate the initial stress σ_0 due to thermal mismatch, and the resulting extrinsic stress σ. Section 4 will present the validation of the proposed theoretical models for the temperature dependent elastic constants with respect to the experimental data. It will also present the 3D simulation results of the thermal induced extrinsic stress σ, obtained from using these elastic constants. This section will also analyze qualitatively and quantitatively these simulation results for σ and provide comparisons with the results found in the literature. Section 5 presents the concluding thoughts and future work.

2. DIFFERENT SOURCES OF INITIAL STRESS

The initial stress σ_0 in the Si(1-x)Ge(x) thin films or in the Silicon substrate depends on many different types of sources as: deposition, oxidation, etching, shallow trench isolation, diffusion, implantation, and neighboring. After deposition, two types of initial stresses will be created in the Si(1-x)Ge(x) thin films: the initial stress due to the lattice mismatch between Si(1-x)Ge(x) and Silicon materials . And, the initial stress due to thermal mismatch. The initial stress σ_0 due to lattice mismatch has been investigated in our previous work (El Boukili 2010). In this paper, we are going to focus on the modeling of the initial stress σ_0 induced by thermal mismatch.

2.1. Initial stress due to lattice mismatch

Right after deposition, thin films are either stretched or compressed to fit the substrate on which they are deposited. The film wants to be smaller if it was stretched earlier, thus creating a tensile initial stress. And, similarly, it creates a compressive initial stress if it was compressed during deposition. The initial stress generated due to this phenomenon can be quantified by Stoney's equation which relates the stress σ_0 to the substrate curvature or by other advanced models (El Boukili 2010).

2.2. Intrinsic stress due to thermal mismatch

Thermal mismatch stress depends on the mechanical properties of the materials. It occurs when two materials with different coefficients of thermal expansion are heated or cooled down. When two different materials are heated or cooled down, they will expand or contract at different rates. During thermal processing, thin film materials like Si(1-x)Ge(x), Poly-Silicon, Silicon Dioxide, or Silicon Nitride expand and contract at different rates compared to the Silicon substrate according to their thermal expansion coefficients. This creates an initial thermal strain and stress in the film and also in the substrate. The deposition takes place at elevated temperatures. When the temperature is

decreased from the fabrication temperature T to the room temperature T0, the volumes of the grains of Si(1-x)Ge(x) films and Silicon substrate shrink and the thermal stresses in the material increase. The initial thermal stress σ_0 in the Si(1-x)Ge(x) films depend mainly on the fabrication temperature T, the elastic constants of Si(1-x)Ge(x), Germanium ratio x, the substrate orientation, the doping, and the deposition technique used. For the current nano PMOS transistors, Si(1-x)Ge(x) films are grown using low pressure chemical vapor deposition (LPCVD), plasma enhanced chemical vapor deposition (PECVD), or Epitaxy. Intel company is using Epitaxial growth for Si(1-x)Ge(x) films.

3. MODELING OF TEMPERATURE EFFECTS ON ELASTIC CONSTANTS OF SILICON AND GERMANIUM

Since the discovery of the transistor in 1947 many research has been done to understand the electrical properties of Silicon (Si) material and other semiconductor materials like Germanium (Ge) or Silicon Germanium (Si(1-x)Ge(x)). However, not enough research has been done to understand the mechanical properties of Si, Ge, and Si(1-x)Ge(x). Between 1947 and 1999 the performances of CMOS transistors were related mainly to the electrical properties of the materials making up the CMOS devices. Only in the beginning of 2000 that Intel discovered that the performances of a nano CMOS transistor can be enhanced dramatically using the mechanical properties of Si, Ge, Si(1-x)Ge(x) or other materials making up the nano NMOS or PMOS transistors (Ghani 2010). The mechanical properties of a material affect significantly its electrical properties. The mechanical properties of Silicon, Germanium, Si(1-x)Ge(x) or any other symmetric material are represented mainly by their elastic constants C11, C12, and C44.

In this paper, we are proposing the following new model which includes the effects of temperature on the elastic constants C11, C12 and C44 to calculate correctly the initial thermal stress $\sigma^0_{SiGe}(T)$ in Si(1-x)Ge(x) thin films:

$$\sigma^0_{SiGe}(T) = D(T).\varepsilon^0_{SiGe}(T) \quad (2)$$

where $\varepsilon^0_{SiGe}(T)$ represents the initial thermal strain tensor which is defined by:

$$\varepsilon^0_{SiGe}(T) = (\varepsilon^{xx}_0, \varepsilon^{yy}_0, \varepsilon^{zz}_0, \varepsilon^{xy}_0, \varepsilon^{yz}_0, \varepsilon^{xz}_0) \quad (3)$$

where $\varepsilon^{xx}_0, \varepsilon^{yy}_0, \varepsilon^{zz}_0$ are the initial normal strain components, and $\varepsilon^{xy}_0, \varepsilon^{yz}_0, \varepsilon^{xz}_0$ are the initial shear strain components that are assumed to be zero. We also assume that in Si(1-x)Ge(x):

$$\varepsilon^{xx}_0 = \varepsilon^{yy}_0 = \varepsilon^{zz}_0 = \varepsilon_{SiGe,0}(T). \quad (4)$$

In our previous work (El Boukili 2015), we have proposed the following model to calculate $\varepsilon_{SiGe,0}(T)$:

$$\varepsilon_{SiGe,0}(T) = \int_{T0}^{T} \alpha_{SiGe}(t)dt + \Delta\alpha(T)\Delta T \quad (5)$$

$$\Delta\alpha(T) = \alpha_{SiGe}(T) - \alpha_{Si}(T), \quad (6)$$

$$\Delta T = T - T0. \quad (7)$$

And the stiffness tensor of elastic constants D(T) is given by the matrix :

$$\begin{bmatrix} c11(T) & c12(T) & c12(T) & 0 & 0 & 0 \\ c12(T) & c11(T) & c12(T) & 0 & 0 & 0 \\ c12(T) & c12(T) & c11(T) & 0 & 0 & 0 \\ 0 & 0 & 0 & c44(T) & 0 & 0 \\ 0 & 0 & 0 & 0 & c44(T) & 0 \\ 0 & 0 & 0 & 0 & 0 & c44(T) \end{bmatrix}$$

As far as we know, no work has been done to include the effects of temperature on the elastic constants to calculate the initial thermal stress σ_0 and the resulting extrinsic stress σ in a nano PMOS transistor. In our previous work (El Boukili 2015), we have used the model given by Equation (1) where the elastic constants C11, C12, and C44 were considered independent of the fabrication temperature T. We have used the values at room temperature T0. We believe that this new model will give more accurate values for the initial thermal stress σ_0 that we need to calculate numerically the resulting extrinsic stress σ in the whole structure of an Intel nano PMOS transistor.

We are proposing and using the following models, based on Taylor's expansion, for the temperature dependence of the elastic constants of Silicon and Germanium materials:

$$C^{Si}_{ij}(T) = C^{Si,0}_{ij}\left[1 + a^{Si}_{ij}(T - T0) + b^{Si}_{ij}(T - T0)^2\right] \quad (8)$$

$$C^{Ge}_{ij}(T) = C^{Ge,0}_{ij}\left[1 + a^{Ge}_{ij}(T - T0) + b^{Ge}_{ij}(T - T0)^2\right]. \quad (9)$$

Where $C^{Si,0}_{ij}$ and $C^{Ge,0}_{ij}$ represent the elastic constants of Silicon and Germanium at room temperature T0. And, $a^{Si}_{ij}, b^{Si}_{ij}, a^{Ge}_{ij}, b^{Ge}_{ij}$ represent the first-order and the second order temperature coefficients of the elastic constants of Silicon and Germanium respectively. Here, the index i is equal to 1and j is equal to 1 or 2. C44 is not needed to calculate the initial stress σ_0.

The values of the Silicon constants $C_{ij}^{Si,o}$, a_{ij}^{Si}, b_{ij}^{Si} are extracted from the measurements values given in (Elding 2015, Antti 2014, Matthew 2010, Bourgeois 1997). The values given in (Antti 2014) are also depending on doping concentrations. In this work, we are taking average values with respect to doping. The results we get for the elastic constants of Silicon ($C_{ij}^{Si}(T)$) are given in Table 1. We believe we are the first to propose and use the model in Equation (9) for Germanium. We should note that not that much work has been done in the literature for Germanium even experimentally.

We are using the least squares method to fit the model in Equation (9) with the measurements from (Madelug 2001) to calculate the values of the constants $C_{ij}^{Ge,o}$, a_{ij}^{Ge}, b_{ij}^{Ge}. The results for $C_{ij}^{Ge}(T)$ are given in Table 1. Finally, to calculate the temperature dependent elastic constants of Si(1-x)Ge(x), we are proposing and using the following model:

$$C_{ij}^{Si(1-x)Ge(x)}(T) = (1-x)C_{ij}^{Si}(T) + xC_{ij}^{Ge}(T). \quad (10)$$

The values we get for $C_{ij}^{Si(1-x)Ge(x)}(T)$ using this model are given in Table 1.

The component form of the initial thermal stress tensor $\sigma_{SiGe}^{o}(T)$, is defined by:

$$\sigma_{SiGe}^{o} = (\sigma_0^{xx}, \sigma_0^{yy}, \sigma_0^{zz}, \sigma_0^{xy}, \sigma_0^{yz}, \sigma_0^{xz}),$$

where $\sigma_0^{xx}, \sigma_0^{yy}, \sigma_0^{zz}$ are the initial normal stress components and $\sigma_0^{xy}, \sigma_0^{yz}, \sigma_0^{xz}$ are the initial shear stress components that are assumed to be zero.

In our simulation program, the thermal initial stress tensor $\sigma_{SiGe}^{o}(T)$ is used as a source term to calculate, in the whole 3D nano PMOS transistor, the extrinsic stress tensor σ defined by: $\sigma = (\sigma^{xx}, \sigma^{yy}, \sigma^{zz}, \sigma^{xy}, \sigma^{yz}, \sigma^{zx})$. We note that σ^{xx}, σ^{yy}, and σ^{zz} represent the extrinsic stress along the channel, vertical to the channel, and across the channel, respectively. This stress σ in the channel is used to enhance the mobility of holes in 3D nano PMOS based on Intel technology (Ghani 2010). We assume that Silicon and Silicon Germanium are elastic materials. And, to calculate the stress tensor σ we use the elastic stress model based on Newton's second law of motion (motion of atoms), and the following extended Hooke's law relating stress to strain:

$$\sigma = D\varepsilon - \sigma_0 + \sigma_{00}. \quad (11)$$

Here σ_{00} is taken to be zero for simplicity. And, σ_0 is the thermal initial stress which is equal to $\sigma_{SiGe}^{o}(T)$ on Si(1-x)Ge(x) films and 0 elsewhere. A detailed description and how to use finite volume method to solve numerically the elastic model (11) in 3D is given in (El Boukili 2010).

4. RESULTS AND VALIDATION

4.1 Validation of the proposed models for elastic constants using experimental data

The following Table 1 summarizes the calculated values of the elastic constants, in GPa, of Si, Ge, and Si(1-x)Ge(x) using the models we proposed in Equations (8),(9), and (10) where x=35% and the temperature is ranging from 25°C to 882°C. The values for the elastic constants of Silicon are in good agreement with measurements from (Antti 2014). The values for the elastic constants of Germanium are in good agreement with the measurements from (Madelug 2001). And those for Si(0.65)Ge(0.35) are in good agreement with the measurements from (Siqing 1992).

Table 1: C11(T) and C12(T) of Si, Ge, and Si(0.65)Ge(0.35) in GPa.

T in °C	Ge: C11;C12	Si(0.65)Ge(0.35): C11;C12	Si: C11;C12
25	124; 41.3	115.08;55.70	164.14;63.46
100	123.36; 40.97	149.36;55.29	163.36;63.00
300	121.18;40.09	146.72;54.10	160.47;61.65
500	118.27;39.17	143.20;52.86	156.62;60.23
700	114.64;38.73	138.80;51.57	151.81;58.77
800	112.55;37.73	136.27;50.91	149.04;58.01
882	110.71;37.32	134.03;50.36	146.60;57.38

We can see from the Table 1 that the values of the elastic constants C11(T) and C12(T) are decreasing with increasing temperature. This will have a significant effect on the mechanical and electrical properties of these materials and also on the performances of the nano CMOS devices using these materials. The values of the elastic constants of Si(0.65)Ge(0.35) in Table 1 are between those of Germanium and Silicon which is in a good agreement with the theory and experiments (Siqing 1992). As far as we know, the models we have proposed in Equations (9) and (10) for Germanium and Si(1-x)Ge(x) are new. No theoretical model has been found in the literature for Germanium and Si(1-x)Ge(x). We believe that not many work has been done for Germanium and Si(1-x)Ge(x) because Silicon is the most employed material in semiconductor industry. Integrated circuits, solar cells, and Micro electro mechanical systems (MEMS) extensively use Silicon and not Germanium or Si(1-x)Ge(x).

4.2 Validation of the proposed models for elastic constants using simulation results of stress

The elastic constants we have calculated in Table 1 are used to calculate the thermal initial stress σ_0 using the Equations (2) and (5). And, we have used this initial stress σ_0 to calculate numerically the resulting extrinsic stress σ, using the Equation (10), in the whole structure of the nano PMOS shown in Figure 1. This PMOS belongs to the 14 nm technology node developed by Intel in 2014. The gate length of this nano PMOS is 23 nm. Its source and drain are made up of Si(0.65)Ge(0.35). The Figure 2 shows the stress distribution along channel (σ^{xx}) when the elastic constants are independent of temperature. The Figure 3 shows the stress distribution along channel when the elastic constants depend on temperature T and T=500°C. Figure 4 shows the stress distribution along channel for T=882°C. From Figure 2, the magnitude of the average value of the stress along channel is 4955e+5 Pa and from Figure 3 the magnitude of the average value of the stress along channel is 4330e+5 Pa. Then, the absolute value of the difference is 625e+5 Pa. And, this is a huge difference. We could then say that the values of stress are overestimated when the effects of temperature are not included in the elastic constants. We can then conclude that to get accurate and correct values of the stress in the channel of a nano PMOS or NMOS transistor, we should take into account the effects of the fabrication temperature on the elastic constants. As far as we know, no work has been done in the past to investigate this crucial issue. From Figures 3 and 4 we could note that the magnitude of the stress along the channel is increasing with increasing temperature.

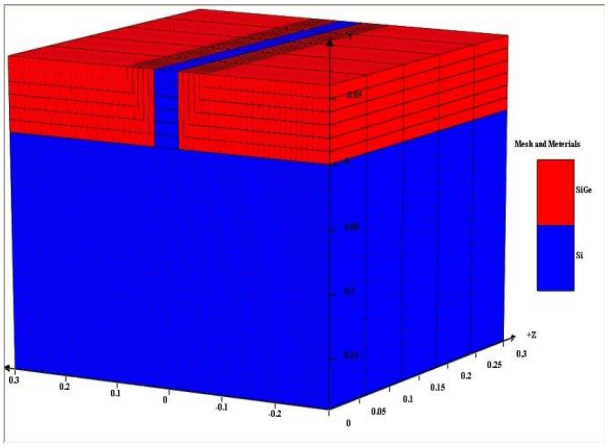

Figure 1: Materials And Mesh Of The Simulated Structure

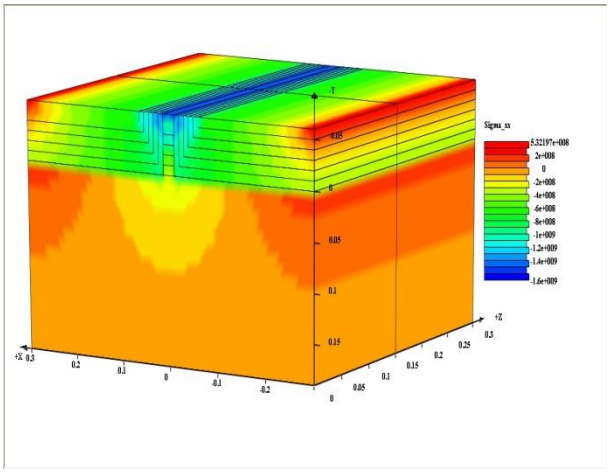

Figure 2: 3D Distribution Of xx Stress Component Without Temperature Effects On C11 And C12

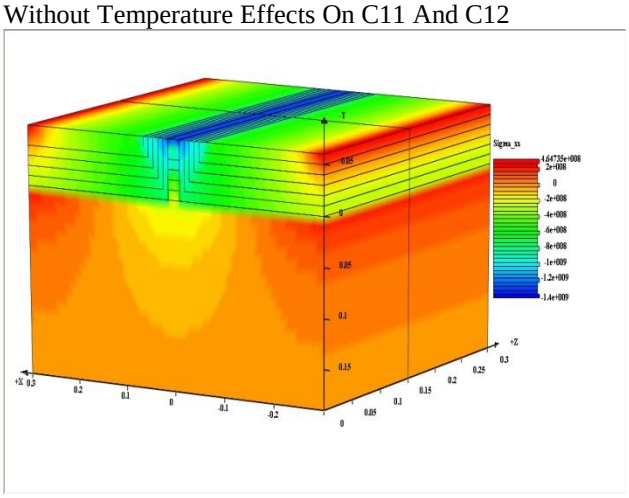

Figure 3: 3D Distribution of xx Stress Component With Temperature Effects On C11 And C12 When T=500°C

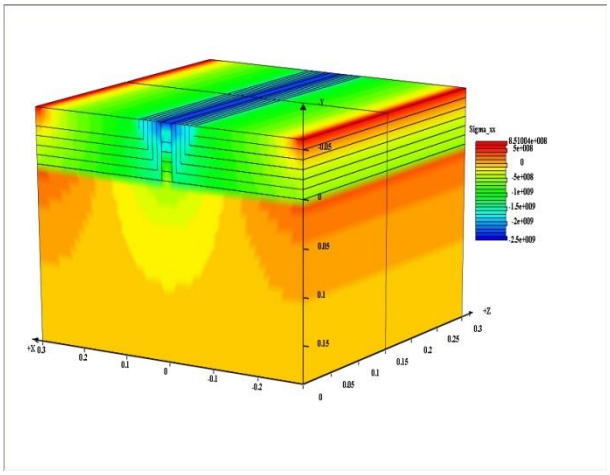

Figure 4: 3D Distribution of xx Stress Component With Temperature Effects On C11 And C12 When T=882°C

5. CONCLUSIONS

In this paper, we have developed new models to calculate accurately the thermal induced initial stress σ_0 and the resulting extrinsic stress σ in the whole structure of the 14nm nano PMOS transistor based on Intel technology. In these models, we have taken into account, for the first time, the effects of the fabrication temperature on the elastic constants C11, and C12of the Silicon, Germanium, and Silicon Germanium. The values of the temperature dependent C11 and C12 obtained with these models are in good agreement with the measurements from (Antti 2014, Madelug 2001, Siqing 1992). The 3D results showing the effects of the fabrication temperature on the extrinsic stress in the whole 14nm nano PMOS transistor are given in the Figures 3 and 4. The obtained values for the extrinsic stress along channel (σ^{xx}) are qualitatively in good agreement with those found in literature (Victor 2013, 2012, 2004) and (El Boukili 2010, 2015). But, quantitatively these values are much smaller than the values given in our previous work (El Boukili 2010, 2015) where the temperature effects were not included in the elastic constants C11 and C12. This is a great finding for nano PMOS and NMOS manufacturers and design engineers. In the future work , we will investigate the effects of doping and temperature on the elastic constants C11 and C12 and explore their effects on the channel stress.

REFERENCES

Antti, J. et al., 2014. Determination of doping and temperature dependent elastic constants of degenerately doped silicon from MEMS resonators. *IEEE Transactions on Ultrasonics, Ferroelectrics, and Frequency Control*, Vol.61, No.7, 1063-1074.

Bera, L.K., 2006. The impact of uniform strain applied via bonding onto plastic substrate on MOSFET performance. *IEEE Electron Device Lett.*, Vol. 27, 58-61.

Bourgeois, C. et al., 1997. Design of resonators for the determination of the temperature coefficients of elastic constants of mono crystalline silicon. *Proceeding of IEEE int. Frequency Control Symp*., pp. 791-799. May 28-30,Orlando, FL,USA.

Chui, K.J., 2007. n-MOSFET with silicon-carbon source/drain for enhancement of carrier transport. *IEEE Trans. Electron Devices*, Vol. 54, 249-256.

Matthew, A. et al., 2010. What's Young modulus of silicon? *Journal of micro electro mechanical systems*, Vol.19, No. 2,229-238.

Madelug, O., Rosser, U., Schulz, M., 2001. *Group IV elements, IV-IV and III-V compounds. Part a-lattice properties.* Volume 41, Berlin Heidelberg: Springer.

El Boukili, A., 2010. 3D Stress simulations of nano transistors. In: Gunther, M., Bartel, A., Brunk, M., Schops, S., Striebel, M., eds. *Progress in Industrial Mathematics at ECMI.* Berlin Heildelberg: Springer, pp. 85-91.

El Boukili, A., 2015. New models for thermal stress simulation in 3D nano CMOS transistors. *Proceedings of the first international conference on electrical and information technologies.* pp. 25-27, March, 25-27, Marrakech, Morocco.

Elding, J.,et al., 2015. Temperature dependence of the elastic constants of doped silicon. Accepted in *Journal of micro electro mechanical systems*.

Ghani, T. et al., 2003. A 90nm high volume Manufacturing Logic Technology Featuring Novel 45nm Gate Length Strained Silicon CMOS Transistors. *Proceedings of IEDM Technical Digest, pp.978-980.* Dec. 8-10, Washington, DC, USA.

Ghani, T., 2010, Challenges and innovations in nano-CMOS transistor scaling. *IEEE workshop on microelectronics and electron device.* April 16, Boise, Idaho, USA.

JianLi, M. et al., 2014. Hole mobility enhancement in uniaxial stressed Ge dependence on stress and transport direction. *Science China, Phys. Mech. & Astr.*, Vol.57, 1860-1865.

Krivokapic, Z. et al., 2003. Locally strained ultra-thin channel 25nm Narrow FDSOI Devices with Metal Gate and Mesa Isolation. *Proceedings of IEDM, IEEE International*, pp. 445-448. Dec. 8-10, Washington, DC, USA.

Siqing, W. et al., 1992. Elastic constants of Si/Ge super lattice and bulk Si and Ge. *Physical Review B*, Volume 46, 12411-12420.

Victor, M., 2004. *Analyzing strained-silicon options for stress-engineering transistors. Solid State Technology Magazine*. July, Vol. 47, issue 7, p49.

Victor, M., et al., 2013. A group IV solution for 7nm FinFET CMOS: Stress engineering using Si,Ge, and Sn. *Proceeding of IEDM*, pp. 26.3.1-26.3.4 Dec. 9-11, Washington, DC, USA.

Victor, M., et al., 2012. 14nm FinFET stress engineering with epitaxial SiGe source/drain. *Proceeding of ISTDM*, pp. 1-2. June 4-6, Berkeley, CA, USA.