MODELLING AND SIMUILATION OF THERMAL INDUCED STRESS IN 3D NANO PMOS

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ABSTRACT
We are presenting a new physically based numerical model in 3D to calculate the intrinsic stress due to thermal mismatch in Silicon Germanium for 3D nanometer PMOSFETs after deposition. This intrinsic stress is used to calculate the extrinsic stress distribution in the channel which has the advantage of enhancing performances of devices and circuits. Numerical results of channel stress based on this novel model will be presented and discussed for Intel 45 nanometers PMOSFETs. Results obtained with this model are in good agreement with those found in literature using other models.

Keywords: workstation modeling and simulation in 3D, physically based model, thermal induced stress, Intel nano PMOSFETs

1. INTRODUCTION

The exponential growth predicted by Moore's Law stayed valid for the last four decades. But, it cannot continue the trend forever. The industry already enters the nanometer regime, where the transistor gate length drops down to 45 nm or below and the gate oxide thickness to 1 nm or below. In this nanometer regime, physical limitations such as off-state leakage current and power density pose a potential threat to enhance performance by simple geometrical scaling. Right now, the industry needs a new scaling vector. Front-end process induced extrinsic stress has thereby emerged as the new scaling vector for the 90 nm node technology and below. The extrinsic stress has the advantage of improving the performances of PMOSFETs and NMOSFETs transistors by the enhancing mobility. This mobility enhancement fundamentally results from alteration of electronic band structure of silicon due to extrinsic stress.

The extrinsic stress is the stress that exits in the whole transistor (or circuit). It is produced by an intrinsic stress that exists in different materials (or films) that make up the transistor. The intrinsic stress is either introduced intentionally or unintentionally or both. The unintentional intrinsic stress is induced by the processing steps as: implantation, etching, deposition of thin films, oxidation, or diffusion. The intentional intrinsic stress is introduced intentionally by the manufacturers to increase performance.

Actually, most of nano semiconductor device manufacturers as Intel, IBM and TSMC are intentionally using the intrinsic stress to produce uniaxial extrinsic stress in the Silicon channel. And, it is now admitted that the channel stress enhances carrier mobilities for both nano PMOS and NMOS transistors (by 30% or more (Krivokapic 2003).

In this paper, we are presenting a new physically based numerical model to calculate the intrinsic stress due to thermal mismatch in Silicon Germanium (SiGe) films after deposition. This intrinsic stress is caused by the different thermal expansion coefficients of the thin films of SiGe and the Silicon (Si) substrate. In fact, the temperature is high during deposition of SiGe films on the top of Si substrate. And, the temperature will cool down to room temperature after deposition. Then, an intrinsic stress will develop in the SiGe thin films and in the Si substrate during the cooling down to room temperature.

This paper is organized as follows. Section 2 will outline different sources of intrinsic stress. Section 3 will present the new physically based model in 3D to calculate the intrinsic stress in SiGe due to thermal mismatch between SiGe and Silicon. Section 4 will present the 3D numerical results of the channel extrinsic stress that is calculated using the intrinsic stress calculated using the proposed model. This section will also analyze qualitatively and quantitatively the numerical results and provide some comparisons with the results found in the literature. Section 5 outlines the concluding thoughts and future work.

2. MA DIFFERENT SOURCES OF INTRINSIC STRESS IN SIGE

The deposition step is the main processing step in determining the intrinsic stress in SiGe films. The deposition takes place at elevated temperatures. When the temperature is decreased, the volumes of the grains of SiGe film shrink and the stresses in the material increase. The stress gradient and the average stress in the SiGe film depend mainly on the Silicon-Germanium ratio, the substrate temperature and orientation, and the deposition technique which is usually LPCVD (low pressure chemical vapor deposition) or PECVD (plasma enhanced chemical vapor deposition). The intrinsic stress existing in thin films has generally the following main sources.

2.1. Intrinsic stress due to lattice mismatch

During deposition, thin films are either stretched or compressed to fit the substrate on which they are deposited. After deposition, the film wants to be smaller if it was stretched earlier, thus creating tensile intrinsic stress. And similarly, it creates a compressive intrinsic stress if it was compressed during deposition. The intrinsic stress generated due to this phenomenon can be quantified by Stoney's equation by relating the stress to the substrate curvature.

2.2 Intrinsic stress due to doping

Boron doping in p-channel source/drain regions introduces a local tensile strain in the substrate due to its size mismatch with Silicon. Boron (B) atom is smaller in size than Silicon atom and when it occupies a substitutional lattice site, a local lattice contraction occurs because the bond length for Si-B is shorter than for Si-Si (Randell 2005, Horn 1955).

It was reported in (Horn 1955) that a single boron atom exerts 0.0141 Angstrom lattice contraction per atomic percentage of boron in Silicon at room temperature. The stress induced in the channel due to boron doping was insignificant for long-channel devices. But, for nanoscale CMOS transistors where the channel lengths are in the nanometer realm, this stress plays a significant role in determining the carrier mobility enhancement.

This tensile stress can be deleterious to the compressive stress intentionally induced by embedded Si(1-x)Ge(x) in source and drain and can result in carrier mobility much lower than expected. Also, the boron solubility in Silicon Germanium increases much beyond its limit in Silicon. So the doping stress generation problem proves to be even more significant in advanced CMOS devices where Germanium concentration is expected to be close to 30%.

Methods to counter and suppress the doping induced stress are very important issues and are still under ongoing research.

2.3 Intrinsic stress due to thermal mismatch

Thermal mismatch stress occurs when two materials with different coefficients of thermal expansion are heated and expand or contract at different rates. During thermal processing, thin film materials like SiGe, Poly-silicon, Silicon Dioxide, or Silicon Nitride expand and contract at different rates compared to the Silicon substrate according to their thermal expansion coefficients. This creates an intrinsic strain and stress in the film and also in the substrate. The thermal expansion coefficient is defined as the rate of change of strain with temperature.

In this paper, we are focusing on the 3D modeling of the intrinsic stress due to thermal mismatch. We are proposing a new second order numerical model. It will be presented and analyzed in the section 3.

3. MODELING OF THERMAL INDUCED INTRINSIC STRESS IN SIGE

Thermal mismatch intrinsic stress occurs when two materials with different coefficients of thermal expansion are heated and expand or contract at different rates. During thermal processing, thin film materials like SiGe, polysilicon, SiO_2, or silicon nitride expand or contract at different rates compared to the Silicon substrate according to their thermal expansion coefficients. The intrinsic strain tensor, ε_0, is defined by:

$$\varepsilon_0 = (\varepsilon_0^{xx}, \varepsilon_0^{yy}, \varepsilon_0^{zz}, \varepsilon_0^{xy}, \varepsilon_0^{yz}, \varepsilon_0^{xz}), \qquad (1)$$

where $\varepsilon_0^{xx}, \varepsilon_0^{yy}, \varepsilon_0^{zz}$ are the intrinsic normal strain components, and $\varepsilon_0^{xy}, \varepsilon_0^{yz}, \varepsilon_0^{xz}$ are the intrinsic shear strain components. We assume that the intrinsic shear strain components are all zero. We also assume that in SiGe:

$$\varepsilon_0^{xx} = \varepsilon_0^{yy} = \varepsilon_0^{zz} = \varepsilon_{SiGe}^{0}(T). \qquad (2)$$

The thermal expansion coefficient of SiGe, $\alpha_{SiGe}(T)$, is defined as the rate of change of the intrinsic strain component, $\varepsilon^0_{SiGe}(T)$, in SiGe with respect to temperature T. Its unit is micro strain/Kelvin (με/K) and it is given by:

$$\alpha_{SiGe}(T) = \frac{d\,\varepsilon^0_{SiGe}(T)}{dT} \qquad (3)$$

Then, the intrinsic strain component will be given by:

$$\varepsilon^{0}{}_{SiGe}(T) = \int_{T0}^{T} \alpha_{SiGe}(t)dt \quad (4)$$

where T0 is the ambient temperature and T is the processing temperature.
For example, T could be the temperature during deposition of SiGe thin film. In this paper, we are choosing $\alpha_{SiGe}(T)$ to be linear with respect to temperature, then our model for intrinsic strain component $\varepsilon^{0}{}_{SiGe}(T)$ given by the equation (4) will be a second order model with respect to temperature T. The models we have found in the literature (Nirav 2005, Freund 2003) are just first order models since they are taking $\alpha_{SiGe}(T)$ as a constant.

On the other hand, to include the effects of the thermal expansion coefficient of the Si substrate, $\alpha_{Si}(T)$, on the intrinsic strain in SiGe thin film, we add the term $\Delta\alpha(T)\Delta T$ to the model given by the equation (4). Then, the proposed model for the intrinsic strain component $\varepsilon^{0}{}_{SiGe}(T)$ is given by:

$$\varepsilon^{0}{}_{SiGe}(T) = \int_{T0}^{T} \alpha_{SiGe}(t)dt + \Delta\alpha(T)\Delta T$$

where

$$\Delta\alpha(T) = \alpha_{SiGe}(T) - \alpha_{Si}(T), \quad (6)$$

$$\Delta T = T - T0. \quad (7)$$

The component form of the intrinsic stress, σ_0, is defined by:

$$\sigma_0 = (\sigma_0^{xx}, \sigma_0^{yy}, \sigma_0^{zz}, \sigma_0^{xy}, \sigma_0^{yz}, \sigma_0^{xz}),$$

(,,)

where $\sigma_0^{xx}, \sigma_0^{yy}, \sigma_0^{zz}$ are the intrinsic normal stress components and $\sigma_0^{xy}, \sigma_0^{yz}, \sigma_0^{xz}$ are the intrinsic shear stress components that are also assumed to be zero. We also assume that in SiGe:

$$\sigma_0^{xx} = \sigma_0^{yy} = \sigma_0^{zz} = \sigma^{0}_{SiGe}(T). \quad (8)$$

On the other hand, we are using a physically based model to define the intrinsic stress tensor σ_0 in the SiGe thin film, since, we are using the Hookean's elastic law to express the relation between strain and stress as follows:

$$\sigma_0 = \begin{bmatrix} \sigma_0^{xx} \\ \sigma_0^{yy} \\ \sigma_0^{zz} \\ \sigma_0^{xy} \\ \sigma_0^{yz} \\ \sigma_0^{xz} \end{bmatrix} = D \cdot \begin{bmatrix} \varepsilon_0^{xx} \\ \varepsilon_0^{yy} \\ \varepsilon_0^{zz} \\ \varepsilon_0^{xy} \\ \varepsilon_0^{yz} \\ \varepsilon_0^{xz} \end{bmatrix}, \quad (9)$$

In three dimensions, the stiffness tensor D, used in our model, for isotropic elastic materials as SiGe is given by:

$$D = \begin{bmatrix} c11 & c12 & c12 & 0 & 0 & 0 \\ c12 & c11 & c12 & 0 & 0 & 0 \\ c12 & c12 & c11 & 0 & 0 & 0 \\ 0 & 0 & 0 & c44 & 0 & 0 \\ 0 & 0 & 0 & 0 & c44 & 0 \\ 0 & 0 & 0 & 0 & 0 & c44 \end{bmatrix} \quad (10)$$

(5)

where the elastic constants c11,c12, and c44 for each material are given by:

$$c11 = \frac{E.(1-\gamma)}{(1+\gamma)(1-2.\gamma)}$$

$$c12 = \frac{E.\gamma}{(1+\gamma)(1-2.\gamma)} \quad (11)$$

$$c44 = \frac{E}{1+\gamma}.$$

The term E represents the Young modulus and the term γ represents the Poisson's ratio. The terms E and γ depend strongly on the material. They depend on the interface's orientation of the substrate that are (001), (110), or (111). For SiGe, they also depend on the Germanium mole fraction.
The model we have found in the literature (Nirav 2005, Freund 2003) for the intrinsic stress component $\sigma^{0}{}_{f}(T)$ is only a 2D model and is given by:

$$\sigma_f^0(T) = (\frac{E}{1-\gamma})(\alpha_f - \alpha_s)\Delta T \ , \qquad (12)$$

where the subscript ‘f’ represents the film, and ‘s’ represents the substrate. The film could be SiGe, Silicon dioxide, Silicon nitride, or another film. We should note that this model is only linear with respect to temperature.

In our simulation program, the intrinsic stress tensor σ_0 is used as a source term to calculate, in the whole 3D nano MOSFET structure, the extrinsic stress tensor $\sigma = (\sigma^{xx}, \sigma^{yy}, \sigma^{zz}, \sigma^{xy}, \sigma^{yz}, \sigma^{zx})$. We note that σ^{xx}, σ^{yy}, and σ^{zz} represent the extrinsic stress along the channel, vertical to the channel, and across the channel. This channel stress is used to enhance the mobility of holes in 3D nano PMOSFETs based on Intel technology (Ghani et al., 2003). We assume that Silicon and Silicon Germanium are elastic materials. And, to calculate the stress tensor σ, we use the elastic stress model based on Newton's second law of motion, and the following Hooke’s law relating stress to strain:

$$\sigma = D\varepsilon + \sigma_0 \ . \qquad (13)$$

Here σ_0 is the intrinsic stress given by the proposed 3D model in the equation (9). A detailed description of this elastic model is given in (El Boukili 2010).

4. 3D NUMERICAL RESULTS AND ANALYSIS

The proposed second order model of intrinsic stress is used to simulate numerically the 3D extrinsic stress in the channel of an Intel 45 nm gate length PMOSFET shown in Figure 1. For the following numerical results, we used (001) for the substrate orientation and 17% as the Germanium mole fraction. In the future, we will do more investigations using different models of temperature.

The results in Figures 2 and 3 show the 3D distribution of x stress components along channel for 300°K and 1000°K respectively. Figure 4 shows 3D distribution of z stress component across channel at 1000°K. This Figure shows also that the stress component σ^{zz} across the channel is also significant. This is an important finding of this paper. A similar stress distribution has been reported in (Victor et al. 2004). The values of the calculated 3D extrinsic stress are also qualitatively and quantitatively in good agreement with those calculated in (Victor et al. 2004). Figure 5 shows the contour lines of the x stress component at 300°K.

All these results did show that the processing temperatures have a great effects on intrinsic and extrinsic stress profiles. These temperature effects will also affect the performances of the MOSFETs devices. On the other hand, these numerical results confirm that our implementation of thermal induced intrinsic and extrinsic stress models in 3D provide valid and correct results. We also believe that these results are of great interest to the semiconductor community including industrials and academia.

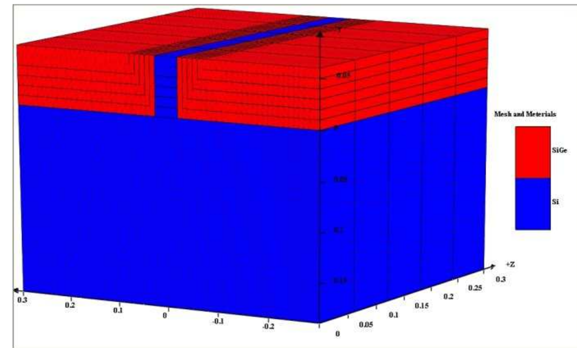

Figure 1: Materials and Mesh of The Simulated Structure

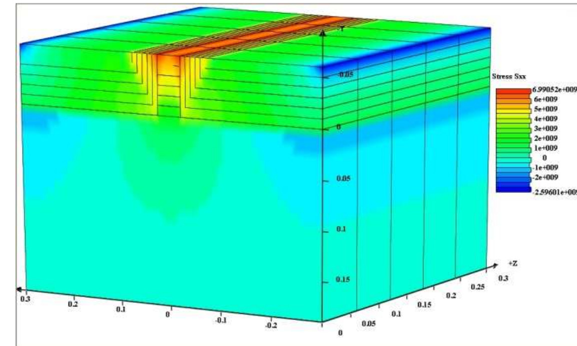

Figure 2: 3D Distribution of x Stress Component Along Channel at 300°K

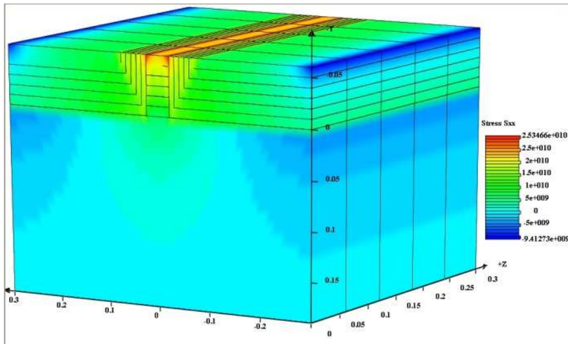

Figure 3: 3D Distribution of x Stress Component Along Channel at 1000°K

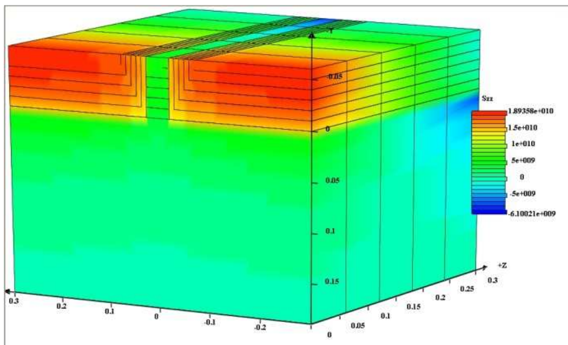

Figure 4: 3D Distribution of z Stress Component Across Channel at 1000°K

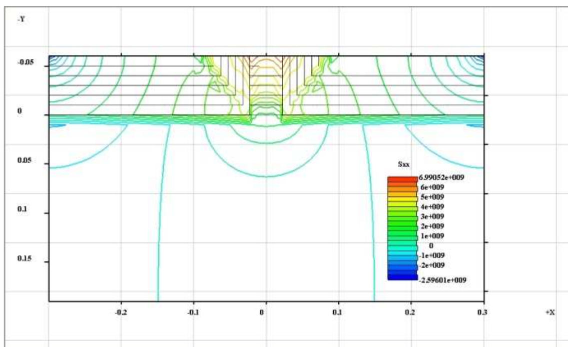

Figure 5: Contour Lines of x Stress Component at 300°K

5. CONCLUSIONS

In this paper, we have developed a new physically based second order model to calculate the intrinsic stress that is due to thermal mismatch between SiGe and Si substrate after deposition of SiGe pockets in source and drain of a strained nano PMOSFETs. This model has been implemented and used successfully to simulate the extrinsic stress in the channel of an Intel 45 nm gate length PMOSFET shown in Figure 1. The important finding of this paper is that all the stress components σ^{xx} and σ^{zz} along the channel, and across the channel respectively are significant. On the other hand, this paper did show that the distribution of the z stress component is really non-uniform in the channel. The quantitative and qualitative behavior of the numerical results is in good agreement with those found in literature (Victor et al. 2004) for similar 3D structure.

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Abderrazzak El Boukili received both the PhD degree in Applied Mathematics in 1995, and the MSc degree in Numerical Analysis, Scientific Computing and Nonlinear Analysis in 1991 at Pierre et Marie Curie University in Paris-France. He received the BSc degree in Applied Mathematics and Computer Science at Picardie University in Amiens-France. In 1996 he had an industrial Post-Doctoral position at Thomson-LCR company in Orsay-France where he worked as software engineer on Drift-Diffusion model to simulate hetero junction bipolar transistors for radar applications. In 1997, he had European Post-Doctoral position at University of Pavia-Italy where he worked as research engineer on software development for simulation and modeling of quantum effects in hetero junction bipolar transistors for mobile phones and high frequency applications. In 2000, he was Assistant Professor and Research Engineer at the University of Ottawa-Canada. Through 2001-2002 he was working at Silvaco Software Inc. in Santa Clara, California-USA as Senior Software Developer on mathematical modeling and simulations of vertical cavity surface emitting lasers. Between 2002-2008, he was working at Crosslight Software Inc. in Vancouver-Canada as Senior Software Developer on 3D Process simulation and Modeling. Since Fall 2008, he is working as Assistant Professor of Applied Mathematics at Al Akhawayn University in Ifrane-Morocco. His main research interests are in industrial TCAD software development for simulations and modeling of opto-electronic devices and processes.
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