IMPROVED LINEARITY CMOS MULTIFUNCTIONAL STRUCTURE USING COMPUTATIONAL CIRCUITS

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ABSTRACT
Original low-power low-voltage multifunctional structure with improved performances will be presented, allowing to implement (with minor changes in the design) two important functions: signal gain with theoretical null distortions and simulation of a perfect linear resistor with positive equivalent resistance. The great advantages of the increased modularity and controllability and of the reduced design costs associated represent an immediate consequence of the multiple functions realized by the proposed structures. The linearity is strongly increased by implementing original techniques, while the silicon occupied area per function is reduced as a result of the proposed multifunctionality. The structures are implemented in $0.35\mu m$ CMOS technology and are supplied at $\pm 3V$. The circuits present a very good linearity (in the worst case, $THD < 0.4\%$), correlated with an extended range of the input voltage (at least $\pm 0.5V$). The tuning range of the active resistors is about hundreds $k\Omega$ - $M\Omega$.

Keywords: Linearity, multifunctionality, computational circuits, VLSI design

1. INTRODUCTION

An important goal in VLSI designs is represented by the possibility of a multiple use for the same cell, the increased modularity that could be achieved being reflected in an important reduction of the design costs per implemented function.
The differential amplifier is an important stage of a large area of applications, including high-performances analog/mixed ICs, such as operational amplifiers, voltage comparators, voltage regulators, video amplifiers, modulators and demodulators or A/D and D/A converters. The linearity of the circuit is relatively poor because of the fundamental nonlinear characteristic of MOS transistors, resulting the possibility of achieving a relatively good linearity only for a restricted input voltage range (the amplitude of the input voltage for the classic differential amplifier using MOS transistors in saturation have to be below a few hundreds of mV). In conclusion, it results the necessity of implementing a linearization technique for decreasing the superior-order nonlinearities of the MOS differential stage and for increasing the available range for the input voltage amplitudes. It exists in literature many circuit techniques used to improve the MOS differential amplifier linearity. It was presented in [1], [2] a third and fifth-order harmonics cancellation with good results and a relatively simple circuit implementation.
A constant-sum of the gate-source voltages circuit connection was described in [3] and it allows an important reduction of the total harmonic distortions coefficient of the circuit. In [4], it was presented and implemented in CMOS technology a simple technique based on square-root circuits for improving the CMOS differential stage linearity, which compensates the quadratic characteristic of the MOS transistor in saturation.
CMOS active resistors are very important blocks in VLSI analog designs, mainly used for replacing the large value passive resistors, with the great advantage of a much smaller area occupied on silicon. Their utilisation domains includes amplitude control in low distortion oscillators, voltage controlled amplifiers and active RC filters. These important applications for programmable floating resistors have motivated a significant research effort for linearising their current-voltage characteristic. The first generation of MOS active resistors [5], [6] used MOS transistors working in the linear region. The main disadvantage is that the realized active resistor is inherently nonlinear and the distortion components were complex functions on MOS technological parameters. A better design of CMOS active resistors is based on MOS transistors working in saturation. Because of the quadratic characteristic of the MOS transistor, some linearization techniques [7], [8] were developed in order to minimize the nonlinear terms from the current-voltage characteristic of the active resistor. An important class of these circuits, referring to the active resistors with controllable negative equivalent resistance, covers a specific area of VLSI designs, finding very large domains of applications such as the canceling of an operational amplifier load or the design of Deboo integrators with improved performances.
The original idea proposed in this paper is to use a linear CMOS differential amplifier for obtaining (with minor changes in the design) two important functions:

- The signal gain with theoretical null distortions;
- Simulation (in a first-order analysis) of a perfect linear resistor using exclusively MOS active devices, having the advantages of a very good controllability of the equivalent resistance and of an important reduction of the silicon occupied

area, especially for large value of the simulated resistance;

2. THEORETICAL ANALYSIS

2.1. Analysis of the classical MOS differential amplifier

The analysis of the large signal operation for the classical MOS differential structure (Fig. 1) can quantitatively evaluate the circuit's nonlinearity, being possible to determine the weight of each superior-order distortion introduced by the structure nonlinearity.

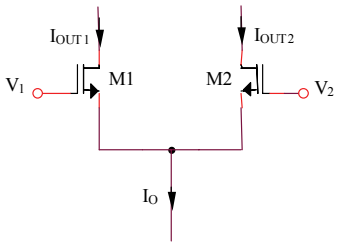

Figure 1: Classical MOS differential structure

The output currents of the classical differential amplifier can be expressed as a function of the differential input voltage as follows:

$$(I_{OUT1})_{1,2} = \frac{I_O}{2} \pm \frac{I_O}{2}\sqrt{\frac{KV^2}{I_O} - \frac{K^2V^4}{4I_O^2}} \quad (1)$$

so:

$$I_{OUT1} = \frac{I_O}{2} + \frac{I_O}{2}\sqrt{\frac{KV^2}{I_O} - \frac{K^2V^4}{4I_O^2}} \quad (2)$$

$$I_{OUT2} = \frac{I_O}{2} - \frac{I_O}{2}\sqrt{\frac{KV^2}{I_O} - \frac{K^2V^4}{4I_O^2}}. \quad (3)$$

The differential output current will be:

$$I_{OUT2} - I_{OUT1} = -\frac{V}{2}\sqrt{4KI_O - K^2V^2}. \quad (4)$$

The $(I_{OUT2} - I_{OUT1})(V)$ function is strongly nonlinear, the quantitative evaluation of the nonlinearity being possible using the Taylor series expansion. The Taylor series expansion of the transfer function (4) can be written as follows:

$$(I_{OUT2} - I_{OUT1})(V) = -K^{1/2}I_O^{1/2}V + \frac{K^{3/2}}{8I_O^{1/2}}V^3 + \frac{K^{5/2}}{128I_O^{3/2}}V^5 + \ldots \quad (5)$$

or:

$$(I_{OUT2} - I_{OUT1})(V) = a_1V + a_3V^3 + a_5V^5 + \ldots \quad (6)$$

a_k being constant coefficients with respect to V differential input voltage. So, as a result of squaring characteristics of MOS transistors biased in saturation, the classical MOS differential amplifier behavior is extremely nonlinear. The first term from (6) is linearly dependent on the input voltage, while the following two terms model the third-order and fifth-order nonlinearities of the differential structure. In conclusion, it is obviously the necessity of implementing a linearization technique for improving the performances of the classical MOS differential stage (good linearity for a relatively extended range for the amplitudes of the input voltage).

2.2. Improved linearity MOS differential structure

An improved linearity MOS differential structure is proposed in Fig. 2. "SQ" block represents a squaring circuit, having the original implementation presented in Fig. 4.

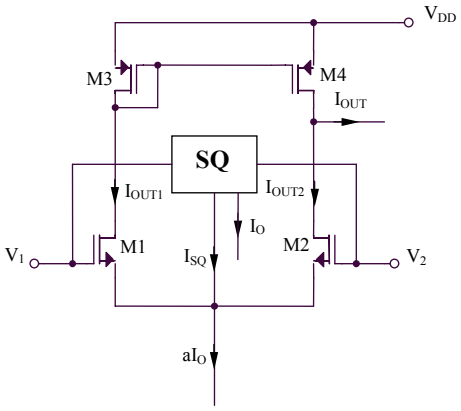

Figure 2: Improved linearity MOS differential structure

The differential output current for this circuit has the following expression:

$$I_{OUT} = (V_1 - V_2)\sqrt{K(aI_O - I_{SQ}) - \frac{K^2}{4}(V_1 - V_2)^2}. \quad (7)$$

In order to obtain a linear behavior of the proposed differential structure, the I_{SQ} output current of the squaring circuit "SQ" must be the sum of a constant term and a term proportional with the square of the differential input voltage:

$$I_{SQ} = bI_O - \frac{K}{4}(V_1 - V_2)^2, \quad (8)$$

b being a positive constant, depending on the particular implementation of the squaring circuit. Replacing (8) in (7), it results:

$$I_{OUT} = \sqrt{(a-b)KI_O}(V_1 - V_2) = G_m(V_1 - V_2) \quad (9)$$

$G_m = \sqrt{(a-b)KI_O}$ being the circuit equivalent transconductance.

2.3. Implementation of the squaring circuit "SQ"

The proposed method for designing the required voltage squaring circuit is based on a differential amplifier (Fig. 3), having a controllable asymmetry between the geometries of its composing transistors. This difference between the aspect ratios of MOS transistors will introduce in the output currents of the differential amplifier a term proportional with the square of the differential input voltage.

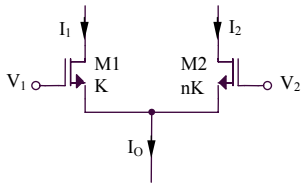

Figure 3: Asymmetrical differential structure

The differential input voltage, V, can be expressed as follows:

$$V = V_{GS1} - V_{GS2} = \sqrt{\frac{2I_1}{K}} - \sqrt{\frac{2(I_O - I_1)}{nK}}, \tag{10}$$

resulting:

$$\frac{K}{2}V^2 = I_1 + \frac{I_O - I_1}{n} - 2\sqrt{\frac{I_1(I_O - I_1)}{n}}. \tag{11}$$

The expression of I_1 current can be obtained solving the following second-order equation, derived from (11):

$$I_1^2\left[\left(\frac{n-1}{n}\right)^2 + \frac{4}{n}\right] + \left(\frac{I_O}{n} - \frac{KV^2}{2}\right)^2 + I_1\left[2\frac{n-1}{n}\left(\frac{I_O}{n} - \frac{KV^2}{2}\right) - \frac{4I_O}{n}\right] = 0 \tag{12}$$

So:

$$I_1 = \frac{I_O}{n+1} + \frac{n(n-1)}{2(n+1)^2}KV^2 + \frac{nV}{(n+1)^2}\sqrt{2KI_O(n+1) - K^2nV^2} \tag{13}$$

and:

$$I_2 = I_O - I_1 = \frac{nI_O}{n+1} - \frac{n(n-1)}{2(n+1)^2}KV^2 - \frac{nV}{(n+1)^2}\sqrt{2KI_O(n+1) - K^2nV^2} \tag{14}$$

The complete realization of a voltage squaring circuit, based on the previous proposed method, uses a cross-coupling of two differential amplifiers having controllable asymmetries between their geometries, M1-M2 and M3-M4 (Fig. 4).

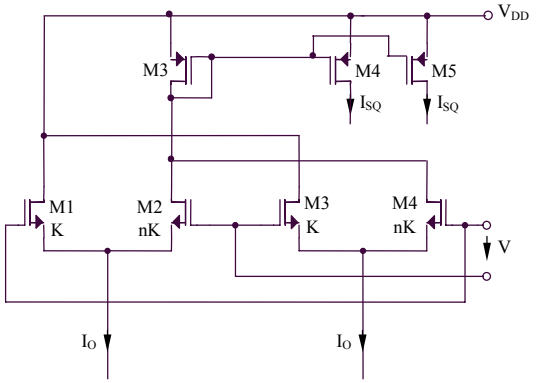

Figure 4: Squaring circuit

Using (13) and (14), it results:

$$I_{SQ} = I_{D2} + I_{D4} = \frac{nI_O}{n+1} - \frac{n(n-1)}{2(n+1)^2}KV^2 - \frac{nV}{(n+1)^2}\sqrt{2KI_O(n+1) - K^2nV^2} + \frac{nI_O}{n+1} - \frac{n(n-1)}{2(n+1)^2}KV^2 + \frac{nV}{(n+1)^2}\sqrt{2KI_O(n+1) - K^2nV^2} = \frac{2nI_O}{n+1} - \frac{n(n-1)}{(n+1)^2}KV^2 \tag{15}$$

2.4. Positive resistance active resistor circuit

The proposed active resistor circuit with positive equivalent resistance is presented in Fig. 5.

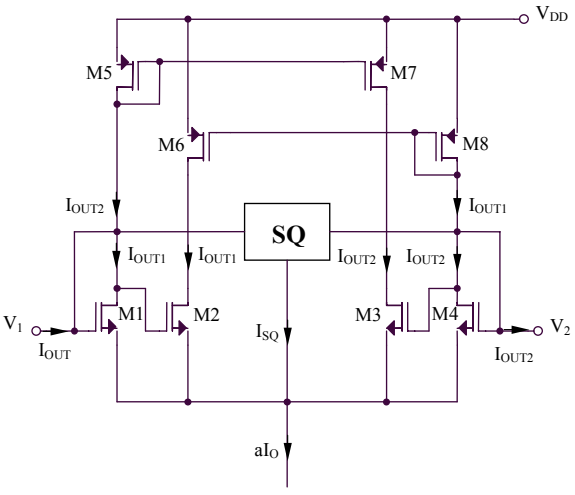

Figure 5: Positive resistance active resistor circuit

The current passing between the input pins V_1 and V_2, $I_{OUT} = I_{OUT1} - I_{OUT2}$ has the following expression:

$$I_{OUT} = (V_1 - V_2)\sqrt{K\frac{aI_O - I_{SQ}}{2} - \frac{K^2}{4}(V_1 - V_2)^2}\ , \quad (16)$$

because each differential amplifier M1-M4 and M2-M3 is biased at a current equal with $I_{OUT1} + I_{OUT2} = (aI_O - I_{SQ})/2$. Using the expression (15) of I_{SQ} current, it results:

$$I_{OUT} = (V_1 - V_2)\sqrt{\begin{matrix}\frac{KI_O}{2}\left(a - \frac{2n}{n+1}\right) + \\ + \frac{K^2(V_1 - V_2)^2}{2}\left[\frac{n(n-1)}{(n+1)^2} - \frac{1}{2}\right]\end{matrix}}\ . \quad (17)$$

The conditions for obtaining a linear behavior of the circuit can be written as $\frac{n(n-1)}{(n+1)^2} = \frac{1}{2}$, resulting $n_{1,2} = 2 \pm \sqrt{5}$ and:

$$I_{OUT} = (V_1 - V_2)\sqrt{\frac{KI_O}{2}\left(a - 2\frac{2 \pm \sqrt{5}}{3 \pm \sqrt{5}}\right)}\ . \quad (18)$$

The equivalent resistance of the circuit presented in Fig. 5 will be:

$$R_{ECH} = \frac{V_1 - V_2}{I_{OUT}} = \left[\frac{KI_O}{2}\left(a - 2\frac{2 \pm \sqrt{5}}{3 \pm \sqrt{5}}\right)\right]^{-1/2}\ . \quad (19)$$

3. SIMULATED RESULTS

The SPICE simulation $I_{OUT1,2}(V)$ based on $0.35\ \mu m$ CMOS technology parameters for the original differential amplifier from Fig. 2 (representing the core of the multifunctional structure) is presented in Fig. 6, showing a very small linearity error. The supply voltage corresponds to low-power requirements, $V_{DD} = 3\ V$.

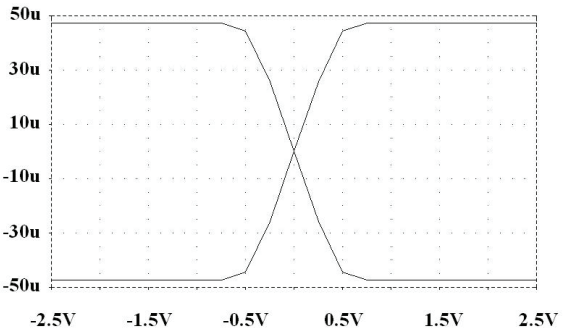

Figure 6: Simulation of the transfer characteristic for the original differential structure

4. CONCLUSIONS

An original low-power low-voltage multifunctional structure with improved performances was presented, allowing to implement (with minor changes in the design) two important functions: signal gain with theoretical null distortions and simulation of a perfect linear resistor with positive equivalent resistance. The great advantages of the increased modularity and controllability and of the reduced design costs associated represent an immediate consequence of the multiple functions realized by the proposed structures. The linearity is strongly increased by implementing original techniques, while the silicon occupied area per function is reduced as a result of the proposed multifunctionality. The structures are implemented in $0.35\mu m$ CMOS technology and are supplied at $\pm 3V$. The circuits present a very good linearity (in the worst case, $THD < 0.4\%$), correlated with an extended range of the input voltage (at least $\pm 0.5V$). The tuning range of the active resistors is about hundreds $k\Omega$ - $M\Omega$.

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