

3D Physics Based Modeling and Simulation of Intrinsic Stress in SiGe for Nano PMOSFETs

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Abstract

We are proposing a new analytical model, in three dimensions, to calculate intrinsic stress that builds during deposition of Silicon Germanium pockets in source and drain of strained nano PMOSFETs. This model has the advantage of accurately incorporating the effects of the Germanium mole fraction and the crystal orientation. This intrinsic stress is used to calculate the extrinsic stress distribution in the channel after deposition. Simulation results of channel stress based on this model will be presented and discussed for Intel technology based nano PMOS transistors.

Keywords: 3D Modeling, Intrinsic Stress, Silicon Germanium, Nano PMOSFETs

1 Introduction

The originality of this paper is the development of new analytical model, in three dimensions (3D), to calculate accurately the intrinsic stress in Silicon Germanium ($Si_{1-x}Ge_x$) due to lattice mismatch between $Si_{1-x}Ge_x$ and Silicon where x represents the Germanium mole fraction. This intrinsic stress is generated during deposition of $Si_{1-x}Ge_x$ pockets in source and drain of Intel nano PMOSFETs (Ghani 2003). In the literature, there are only few papers and only in two dimensions (2D) about the modeling of intrinsic stress in SiGe (Rieger and Vogl 1993; Van de Walle and Martin 1986; Fischetti and Laux 1996; Brash, Dewey, Doczy, and Doyle 2004). These papers were developed in the context of device simulations for mobility modeling under the effects of stress. On the other hand, in most advanced commercial or noncommercial process simulators as FLOOPS, Sentaurus, or Athena,

the intrinsic stress is a user defined input. And, it is not calculated internally by the simulator.

In this paper, we are attempting to extend the 2D models found in the literature to 3D in the context of process simulation. We are following the 2D model of Van de Walle (Van de Walle and Martin 1986).

Most of nano semiconductor device manufacturers as Intel, IBM and TSMC are intentionally using this intrinsic stress to produce uniaxial extrinsic stress in the Silicon channel. And, it is now admitted that the channel stress enhances carrier mobilities for both nano PMOS and NMOS transistors by up to 30% (Krivokapic 2003).

The need of the hour is the development of accurate physics based models and the use of TCAD simulation tools to understand the physics of intrinsic and extrinsic stress and how to attain the desired stress in the channel.

This paper is organized as follows. Section 2 outlines the different sources of intrinsic stress in $Si_{1-x}Ge_x$ pockets generated during deposition. Section 3 describes the proposed 3D model to calculate accurately the intrinsic stress due to lattice mismatch between $Si_{1-x}Ge_x$ and Silicon. After deposition process, intrinsic stress produces an extrinsic stress distribution in the whole device. This section, also outlines the 3D elastic model for the extrinsic stress and how it is related to the intrinsic stress. Section 4 presents 3D simulation results and analysis of extrinsic stress distribution in 45nm Intel strained PMOSFETs (Ghani 2003) using the proposed intrinsic model. This section will also present 3D numerical results showing the effects of Germanium (Ge) mole fractions and crystal orientations on the intrinsic stress. For qualitative and quantitative validations, the channel extrinsic stress profiles will be calculated using the proposed 3D intrinsic stress model and will

be compared with channel stress profiles found in the literature.

At this point, we could not find any experimental values of intrinsic stress in 3D. Therefore, we could not provide any comparisons with experiments.

2 Sources of intrinsic stress in SiGe

The deposition process plays a key role in determining the intrinsic stress in $Si_{1-x}Ge_x$ films. At first, we should note that the deposition takes place at elevated temperatures. When the temperature is decreased, the volumes of the grains of $Si_{1-x}Ge_x$ film shrink and the stresses in the material increase. The stress gradient and the average stress in the $Si_{1-x}Ge_x$ film depend mainly on the Silicon-Germanium ratio, the substrate temperature and orientation, and the deposition technique which is usually LPCVD (low pressure chemical vapor deposition) or PECVD (plasma enhanced chemical vapor deposition). It was observed that the average stress becomes more compressive, if the Ge concentration decreases (Hollauer 2007). Thus, it is expected that a film with higher Ge concentration has a higher degree of crystallinity and larger grains, which leads to higher film density and to higher intrinsic stress. The intrinsic stress observed in thin films has generally the following main sources.

2.1 Intrinsic stress due to lattice mismatch

During deposition, thin films are either stretched or compressed to fit the substrate on which they are deposited. After deposition, the film wants to be smaller if it was stretched earlier, thus creating tensile intrinsic stress. And similarly, it creates a compressive intrinsic stress if it was compressed during deposition. In this paper, we are focusing on developing an analytical model in 3D for this type of intrinsic stress.

2.2 Intrinsic stress due to thermal mismatch

Thermal mismatch stress occurs when two materials with different coefficients of thermal expansion are heated and expand/contract at different rates. During thermal processing, thin film materials like $Si_{1-x}Ge_x$, Polysilicon, Silicon Dioxide, or Silicon Nitride expand and contract at different rates compared to the Silicon

substrate according to their thermal expansion coefficients. This creates an intrinsic strain and stress in the film and also in the substrate. The thermal expansion coefficient is defined as the rate of change of strain with temperature.

2.3 Intrinsic stress due to dopant

Boron doping in p-channel source/drain regions introduces a local tensile strain in the substrate due to its size mismatch with Silicon. Boron (B) atom is smaller in size than Silicon atom and when it occupies a substitutional lattice site, a local lattice contraction occurs because the bond length for Si-B is shorter than for Si-Si (Randell 2005, Horn 1955). We will deal with the 3D modeling of intrinsic stress due thermal mismatch and doping in future work.

3 Proposed 3D analytical model

In this section, we are going to describe the proposed analytical model in 3D to calculate the three normal components ($\sigma_0^{xx}, \sigma_0^{yy}, \sigma_0^{zz}$) of the intrinsic stress in $Si_{1-x}Ge_x$ due to lattice mismatch at the interfaces between Silicon and Silicon Germanium.

We did follow the same strategy used in the 2D model of Van de Walle (Van de Walle and Martin 1986). We first calculate the strained lattice constants parallel and perpendicular to the interfaces in x , y and z directions. Then, from these lattice constants, we calculate the strain parallel and perpendicular to the interfaces in x , y and z directions. And, finally, we get the 3 normal stress components in 3D from the calculated strain using a modified Hookes's law. The restriction of the proposed 3D model to 2D gives exactly the 2D model of Van de Walle. And, this is a great advantage for validations and even comparison issues.

In 3D PMOSFET with SiGe source and drain as shown in the Figure 2, there are two interfaces between Si and SiGe: a vertical interface and a horizontal interface. In the Figure 2, the vertical interface is defined in the yz -plane and the horizontal interface is defined in the xz -plane. Let's assume that $Si_{1-x}Ge_x$ pocket grown in source or drain area has thickness D_{SiGe}^h and D_{SiGe}^v at horizontal and vertical interface respectively. Let D_{Si}^h and D_{Si}^v be the thickness of the Silicon substrate at horizontal and vertical interface respectively. Strains will be generated due to lattice mismatch of

the lattice constants. Let A_{Si} and A_{SiGe} be the lattice constants of unstrained Silicon and $Si_{1-x}Ge_x$. Let $A_{\parallel,h,x}^i$, $A_{\parallel,h,z}^i$ and $A_{\parallel,v,y}^i$ be the strained lattice constants parallel to the horizontal interface in x and z directions and parallel to vertical interface in y direction. The index i represents the Silicon or Silicon Germanium materials. Let $A_{\perp,h,x}^i$, $A_{\perp,h,z}^i$, and $A_{\perp,v,y}^i$, be the strained lattice constants perpendicular to the horizontal interfaces in x and z directions and perpendicular to the vertical interface in y direction. Please see Figure 1 to have an idea about the lattice constants parallel and perpendicular to a given interface between Silicon and Silicon Germanium.

In 2D, Van de Walle assumed that $A_{\parallel,h,x}^{Si} = A_{\parallel,h,x}^{SiGe}$ and $A_{\parallel,v,y}^{Si} = A_{\parallel,v,y}^{SiGe}$. In 3D, we are also assuming that $A_{\parallel,h,z}^{Si} = A_{\parallel,h,z}^{SiGe}$. For simplicity, let's assume that $A_{\parallel,x} = A_{\parallel,h,x}^i$, $A_{\parallel,z} = A_{\parallel,h,z}^i$, and $A_{\parallel,y} = A_{\parallel,v,y}^i$. The 2D model of Van de Walle gave expressions to calculate the strained lattice constants parallel and perpendicular to the interfaces in x , y directions. For the interface in z direction, we use the same expression given by:

$$A_{\parallel,z} = \frac{(A_{Si}G_{Si}^z D_{Si}^h + A_{SiGe}G_{SiGe}^z D_{SiGe}^h)/(G_{Si}^z D_{Si}^h + G_{SiGe}^z D_{SiGe}^h)}{1}$$

$$A_{\perp,h,z}^i = A_i[1 - D_i^z(\frac{A_{\parallel,z}}{A_i} - 1)]$$

The shear modulus G_i^z for Silicon and SiGe depend on the elastic constants of the material i and depend on the the orientation of interface in z direction. It is given by:

$$G_i^z = 2(C_{11}^i + 2C_{12}^i)(1 - \frac{D_i^z}{2})$$

In this paper, the constant D_i^z depend on the elastic constants $C_{11}^i, C_{12}^i, C_{44}^i$ of each material i . And, they also depend on the interfaces's orientations that are (001), (110), or (111). In this work, the elastic constants C_{11}, C_{12}, C_{44} for $Si_{1-x}Ge_x$ depend on the Germanium mole fraction x and on the elastic constants C_{11}, C_{12}, C_{44} of Silicon and Germanium that we get from Van Der Walles Table I. We are going to use a nonlinear extrapolation method of (Rieger and Vogl 1993) to calculate C_{11}, C_{12} , and C_{44} for $Si_{1-x}Ge_x$. We calculate the constant D_i^z that depends on the orientation of the interface in z direction by following the 2D model of (Fischetti and Laux 1996; Van de

Walle and Martin 1986):

$$\begin{aligned} D_{i,(001)}^z &= \frac{2C_{12}^i}{C_{11}^i} \\ D_{i,(110)}^z &= \frac{C_{11}^i + 3C_{12}^i - 2C_{44}^i}{C_{11}^i + C_{12}^i + 2C_{44}^i} \\ D_{i,(111)}^z &= \frac{C_{11}^i + 3C_{12}^i - 2C_{44}^i}{C_{11}^i + C_{12}^i + C_{44}^i} \end{aligned} \quad (1)$$

The ratio of strained lattice constants $A_{\parallel,x}, A_{\parallel,y}, A_{\parallel,z}$ and $A_{\perp,h,x}^i, A_{\perp,v,y}^i$, and $A_{\perp,h,z}^i$ to unstrained lattice constants A_i determines the intrinsic strain parallel and perpendicular to the interfaces in x , y , and z directions: $(\epsilon_{\parallel,h,x}, \epsilon_{\perp,h,x}, \epsilon_{\parallel,v,y}, \epsilon_{\perp,v,y}, \epsilon_{\parallel,h,z}, \epsilon_{\perp,h,z})$. At horizontal interfaces in x and z directions, and at vertical interface in y direction, we have:

$$\epsilon_{\parallel,h,x} = (\frac{A_{\parallel,x}}{A_{SiGe}} - 1), \quad \epsilon_{\perp,h,x} = (\frac{A_{\perp,h,x}^i}{A_{SiGe}} - 1)$$

$$\epsilon_{\parallel,h,z} = (\frac{A_{\parallel,z}}{A_{SiGe}} - 1), \quad \epsilon_{\perp,h,z} = (\frac{A_{\perp,h,z}^i}{A_{SiGe}} - 1)$$

$$\epsilon_{\parallel,v,y} = (\frac{A_{\parallel,y}}{A_{SiGe}} - 1), \quad \epsilon_{\perp,v,y} = (\frac{A_{\perp,v,y}^i}{A_{SiGe}} - 1)$$

Let $\sigma_0^{xx,h,x}, \sigma_0^{zz,h,z}, \sigma_0^{xx,v,y}$ and $\sigma_0^{yy,v,y}$ be the intrinsic stress at the horizontal interface in x and z directions and at the vertical interface in y direction respectively. We use a modified Hookes's law to get these intrinsic stress components from the intrinsic strains as follows:

$$\sigma_0^{xx,h,x} = (C_{11} + C_{12})\epsilon_{\parallel,h,x} + C_{12}(\epsilon_{\perp,h,x} + \epsilon_{\parallel,h,z})$$

$$\sigma_0^{zz,h,z} = E\epsilon_{\perp,h,z}$$

$$\sigma_0^{yy,v,y} = (C_{11} + C_{12})\epsilon_{\parallel,v,y} + C_{12}(\epsilon_{\perp,v,y} + \epsilon_{\parallel,h,z})$$

$$\sigma_0^{xx,v,y} = E\epsilon_{\perp,v,y}$$

The elastic constants C_{11}, C_{12} and the Young's modulus E are those of $Si_{1-x}Ge_x$. Finally, the normal intrinsic stress components $\sigma_0^{xx}, \sigma_0^{yy}$, and σ_0^{zz} in $Si_{1-x}Ge_x$ in the proposed 3D model are calculated as follows:

$$\sigma_0^{xx} = \sigma_0^{xx,h,x} + \sigma_0^{xx,v,y}$$

$$\sigma_0^{yy} = \sigma_0^{yy,v,y} \quad (2)$$

$$\sigma_0^{zz} = \sigma_0^{zz,h,z}$$

We should note that the proposed 3D model given by the equations (2) reduces to 2D model of Van de Walle if we take $\sigma_0^{zz,h,z} = 0$ and $\epsilon_{\parallel,h,z} = 0$. The 3 shear intrinsic stress

components σ_0^{xy} , σ_0^{yz} , and σ_0^{zx} are taken to be zero. Then, the 6 components of the intrinsic stress tensor σ_0 in $Si_{1-x}Ge_x$ are given by: $\sigma_0 = (\sigma_0^{xx}, \sigma_0^{yy}, \sigma_0^{zz}, 0, 0, 0)$.

The intrinsic stress tensor σ_0 is used as a source term to calculate, in the whole 3D nano MOSFET structure, the extrinsic stress tensor $\sigma = (\sigma^{xx}, \sigma^{yy}, \sigma^{zz}, \sigma^{xy}, \sigma^{yz}, \sigma^{zx})$. We note that σ^{xx} , σ^{yy} , and σ^{zz} represent the extrinsic stress along the channel, vertical to the channel, and across the channel. We assume that Silicon and Silicon Germanium are elastic materials. And, to calculate the stress tensor σ , we use the elastic stress model based on Newton's second law of motion, and the following Hookes law relating stress to strain: $\sigma = D(\epsilon - \epsilon_0) + \sigma_0$. Here D is the tensor of elastic constants C_{11}, C_{12}, C_{44} , $\epsilon_0 = 0$ is the intrinsic strain and σ_0 is the intrinsic stress given by the equations (2). A detailed description of this elastic model is given in (El Boukili 2011).

Table 1: Ge Mole Fraction Effects on Stress

Ge%	σ_0^{xx}	σ_0^{yy}	σ_0^{zz}
17	$-1.432e^{10}$	$3.269e^9$	$1.752e^9$
20	$-1.674e^{10}$	$3.821e^9$	$2.047e^9$
30	$-2.454e^{10}$	$5.607e^9$	$3.000e^9$
40	$-3.197e^{10}$	$7.312e^9$	$3.914e^9$
50	$-3.900e^{10}$	$9.321e^9$	$4.780e^9$

Table 2: Substrate Orientation Effects on Stress

Orientation	σ_0^{xx}	σ_0^{yy}	σ_0^{zz}
(100)	$-8.859e^9$	$1.186e^{10}$	$6.361e^9$
(110)	$-1.432e^{10}$	$3.269e^9$	$1.752e^9$
(111)	$-1.556e^{10}$	$1.327e^9$	$7.116e^8$

4 3D Numerical Results and Analysis

The proposed 3D model for intrinsic stress given by the equations (2) is used to simulate numerically the 3D extrinsic stress in the channel of an Intel 45nm gate length PMOSFET shown in Figure 2. For the following numerical results we used (001) for the substrate orientation and 17% as the Germanium mole fraction. In the future, we will do more investigations using different gate lengths (32nm, 22nm and below), different substrate orientations and Germanium mole fractions. The Table 1 shows the effects of Germanium mole fraction on the intrinsic stress

in $Si_{1-x}Ge_x$. From Table 1, we observe that the intrinsic stress along channel becomes more compressive, if the Ge concentration decreases. This is in great agreement with what was reported in (Hollauer 2007). Table 2 show the effects of substrate orientations on the intrinsic stress. The results in Figures 3 and 4 show that the stress components σ_{xx} and σ_{zz} along the channel, and across the channel respectively are all significant. A similar stress distribution has been reported in (Victor 2004). The values of the calculated 3D extrinsic stress are also qualitatively and quantitatively in good agreement with those calculated in (Victor 2004).

Figure 5 shows that the distribution of x stress component is compressive along channel as expected. Figure 6 shows that the distribution of the z stress component is really nonuniform in the channel. A similar result was reported in (Victor 2004). These numerical results confirm that our implementation of intrinsic and extrinsic stress models in 3D provide valid and correct results. We also believe that these results are of great interest to the semiconductor community including industrials and academia.

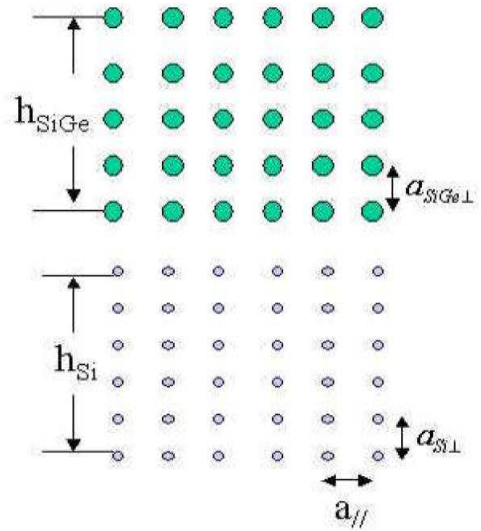


Figure 1: Parallel and perpendicular strained lattice constants.

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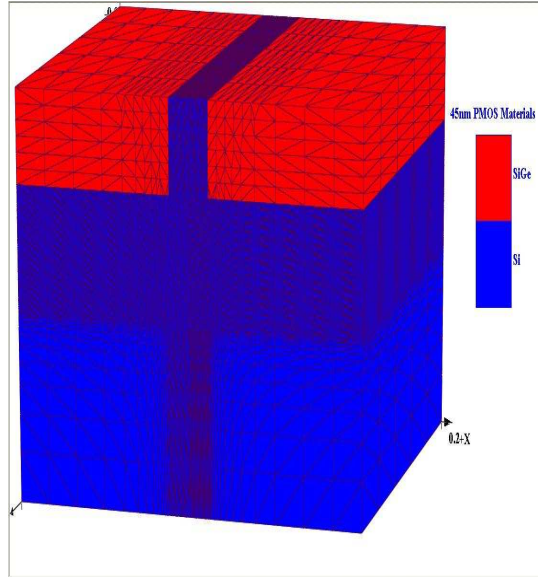


Figure 2: Materials and mesh of the simulated structure.

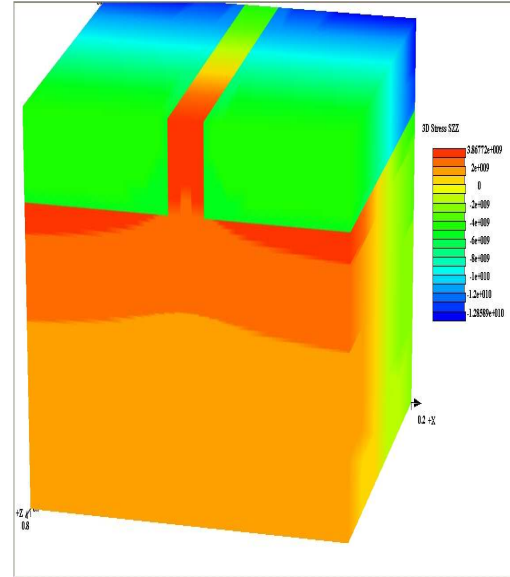


Figure 4: 3D distribution of z stress component across channel.

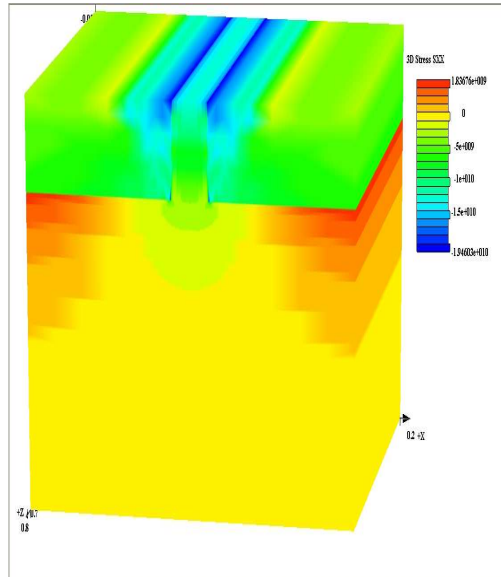


Figure 3: 3D distribution of x stress component along channel.

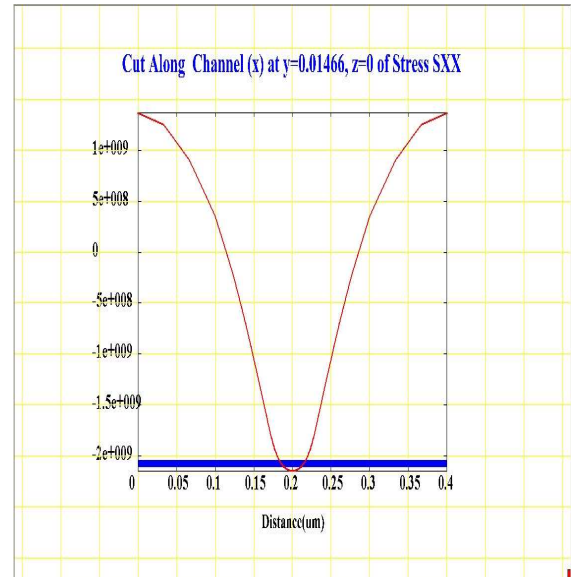


Figure 5: Cut along channel of x stress component.

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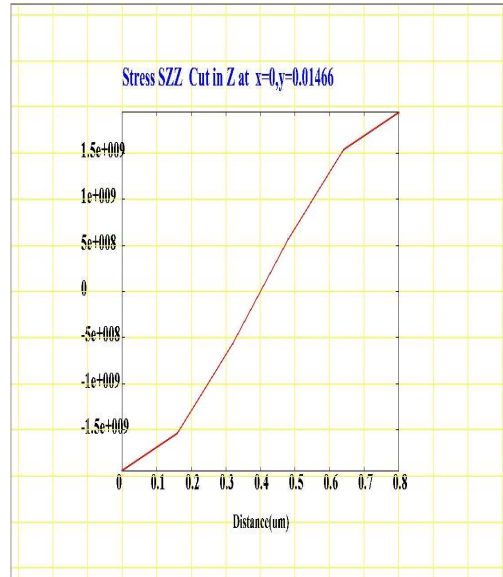


Figure 6: Cut in z-direction of z stress component.

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