CONTROLLABLE EQUIVALENT RESISTANCE CMOS ACTIVE RESISTOR WITH IMPROVED ACCURACY AND INCREASED FREQUENCY RESPONSE

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ABSTRACT

A new active resistor circuit will be further presented. The main advantages of the original proposed implementation are the improved linearity, the small area consumption and the improved frequency response. An original technique for linearizing the $I(V)$ characteristic of the active resistor will be proposed, based on the simulation of the Ohm law using two linearized differential amplifiers, a multiplier and a current-pass circuit. The controllability of the active resistor circuit is excellent, existing the possibility of modifying the value of the equivalent resistance by changing the ratio between a control voltage and a control current. Additionally, the value of the simulated resistance is not function on technological parameters, with the result of improved circuit accuracy. The errors introduced by the second-order effects will be also strongly reduced, while the area consumption of the active resistor will be minimized by replacing the classical MOS transistor with FGMOS (Floating Gate MOS) devices.

Keywords: active resistor, differential amplifiers, linearity error, second-order effects

I. INTRODUCTION

CMOS active resistors are very important blocks in VLSI analog designs, mainly used for replacing the large value passive resistors, with the great advantage of a much smaller area occupied on silicon. Their utilization domains includes amplitude control in low distortion oscillators, voltage controlled amplifiers and active RC filters. These important applications for programmable floating resistors have motivated a significant research effort for linearising their current-voltage characteristic.

The first generation of MOS active resistors [1], [2] used MOS transistors working in the linear region. The main disadvantage is that the realised active resistor is inherently nonlinear and the distortion components were complex functions on MOS technological parameters.

A better design of CMOS active resistors is based on MOS transistors working in saturation [3], [4], [5]. Because of the quadratic characteristic of the MOS transistor, some linearisation techniques were developed in order to minimize the nonlinear terms from the current-voltage characteristic of the active resistor. Usually, the resulting linearisation of the $I-V$ characteristic is obtained by a first-order analysis. However, the second-order effects which affect the MOS transistor operation (mobility degradation, bulk effect and short-channel effect) limits the circuit linearity introducing odd and even-order distortions, as shown in [4]. For this reason, an improved linearisation technique has to be design to compensate the nonlinearities introduced by the second-order effects.

II. THEORETICAL ANALYSIS

The original idea for implementing a linear current-voltage characteristic of the active resistor, similar to the characteristic of a classical passive resistor is to simulate the Ohm law using two linearized differential amplifiers and a multiplier circuit. Because of the requirements for a good frequency response, only MOS transistors working in saturation could be used.

2.1. The block diagram of the active resistor

The structure of the proposed active resistor is based on four important blocks: two differential amplifiers *AD1* and *AD2* with linear transfer function, a multiplier circuit *MULT* and a current-pass circuit I, the block diagram being presented in Figure 1.

The I_{XY} current, which is passing through the I block, is generated by the multiplier circuit, $I_{XY} = I_O I_2 / I_1$, while I_1 and I_2 currents are obtained from the differential amplifiers *AD1* and *AD2*, $I_1 = g_{m1} V_O$ and $I_2 = g_{m2}(V_X - V_Y)$. It results:

$$I_{XY} = I_O \frac{g_{m2}}{g_{m1}} \frac{V_X - V_Y}{V_O}. \quad (1)$$

The equivalent resistance of the circuit having the block diagram presented in Figure 1 will be:

$$R_{ech.} = \frac{V_X - V_Y}{I_{XY}} = \frac{V_O}{I_O} \frac{g_{m1}}{g_{m2}} = \frac{V_O}{I_O} \sqrt{\frac{(W/L)_1}{(W/L)_2} \frac{I_{O1}}{I_{O2}}}. \quad (2)$$

The great advantage of the proposed implementation of the active resistor is the very good controllability of the equivalent resistance by the ratio of a control voltage V_O and a control current I_O. As it is shown in (2), the value of the resistance does not depend on technological parameters, $(W/L)_1$ and $(W/L)_2$ representing aspect ratios of the transistors composing the differential

amplifiers *AD1* ad *AD2*, respectively, while I_{O1} and I_{O2} being biasing currents of these amplifiers.

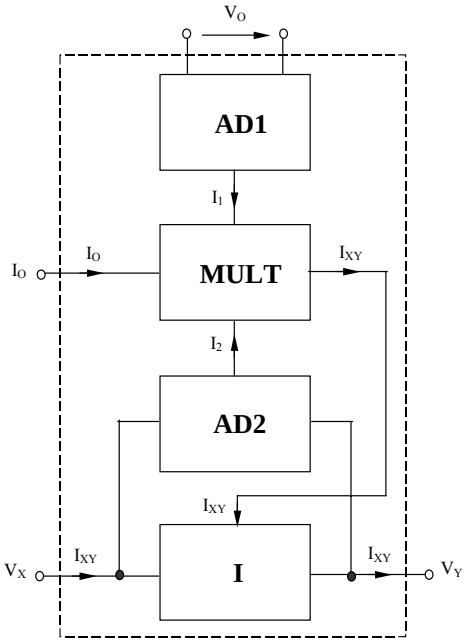

Figure 1: The block diagram of the active resistor

2.2. Classical CMOS differential amplifier

The most common approach of a differential amplifier in CMOS technology is based on strong-inverted MOS transistors (usually working in the saturation region), having the most important advantage of a much better frequency response with respect to the weak-inverted MOS differential amplifiers. As a result of the quadratic characteristic of a MOS transistor operating in saturation, the transfer characteristic of the classical CMOS differential amplifier will be strongly nonlinear, its linearity being in reasonable limits only for a very limited range of the differential input voltage. The drain currents of the classical CMOS differential amplifier will have the following nonlinear dependence on the differential input voltage, v_{id} :

$$I_{d_{1,2}} = \frac{I_O}{2} \pm \frac{I_O}{2}\left(\frac{Kv_{id}^2}{I_O} - \frac{K^2 v_{id}^4}{4I_O^2}\right)^{1/2}, \qquad (3)$$

having a Taylor expansion around $v_{id} = 0$, fifth-order limited expressed by:

$$I_{d_{1,2}}(v_{id}) \cong \frac{I_O}{2} \pm \frac{K^{1/2} I_O^{1/2}}{2} v_{id} \mp \frac{K^{3/2}}{16 I_O^{1/2}} v_{id}^3 \mp .., \qquad (4)$$

where I_O is the biasing current for the differential amplifier. In order to improve the circuit linearity, especially for large values of the differential input voltage (*THD* has relatively large values for v_{id} of about hundreds of *mV*), a linearization technique has to be implemented.

2.3. The original linearized differential amplifier

The original proposed differential structure from Figure2 is based on a symmetrical structure that assures, in a first-order analysis, the linearization of the transfer characteristic, equivalent to a constant circuit transconductance.

Supposing a saturation operation of all MOS active devices from the previous circuit, it is possible to write that the output current expression is $I_2 = I_X - I_Y$:

$$I_2 = \frac{K}{2}\left(V_{GS_X} - V_{GS_Y}\right)\left(V_{GS_X} + V_{GS_Y} - 2V_T\right). \qquad (5)$$

Because:

$$V_{GS_X} - V_{GS_Y} = 2\left(V_X - V_Y\right) \qquad (6)$$

and:

$$V_{GS_X} + V_{GS_Y} = 2V_{GS_O}, \qquad (7)$$

it results a linear dependence of the output current on the differential input voltage:

$$I_2 = \sqrt{8KI_O}\left(V_X - V_Y\right), \qquad (8)$$

equivalent to a constant transconductance of the circuit:

$$g_m = \sqrt{8KI_O}. \qquad (9)$$

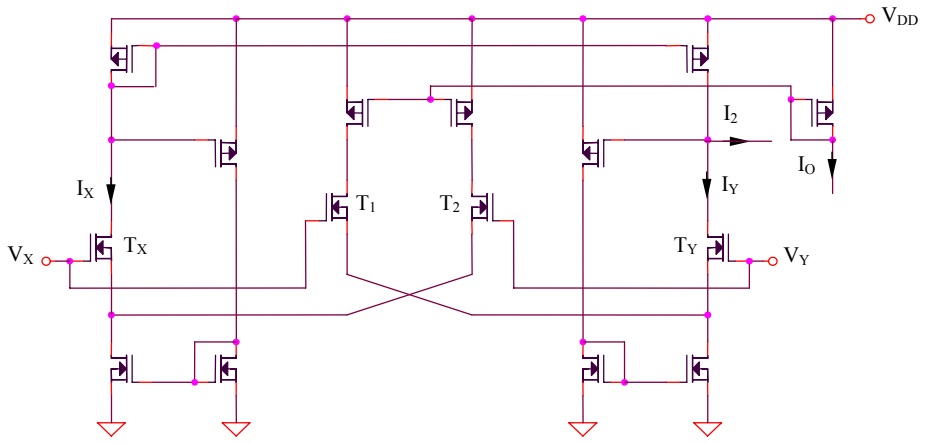

Figure 2: The linearized differential structure

The important advantages of the previous circuit is the improved linearity that could be achieved in a first-order analysis and the possibility of controlling the value of the transconductance by modifying a continuous current (I_O).

2.4. The second-order effects

The linearity (8) of the transfer characteristic of the differential amplifier from Figure 2 is slightly affected by the second-order effects that affect the MOS transistor operation, modeled by the following relations: channel-length modulation (10) and mobility degradation (11)).

$$I_D = \frac{K}{2}(V_{GS} - V_T)^2(1 + \lambda V_{DS}) \tag{10}$$

$$K = \frac{K_0}{[1 + \theta_G(V_{GS} - V_T)](1 + \theta_D V_{DS})}. \tag{11}$$

Considering that the design condition $\lambda = \theta_D$ is fulfilled, the gate-source voltage of a MOS transistor working in saturation at a drain current I_D will be:

$$V_{GS} = V_T + \sqrt{\frac{2I_D}{K}} + \theta_G \frac{I_D}{K}. \tag{12}$$

The last term represents the error which affects the quadratic characteristic of the MOS transistor biased in saturation, caused by the previous presented second-order effects. The result will be a small accuracy degradation of the entire circuit linearity, quantitative evaluated by the superior-order terms in the transfer characteristic of the differential amplifier:

$$I_{XY} = \sum_{k=1}^{\infty} a_k (V_X - V_Y)^k. \tag{13}$$

Because of the circuit symmetry, the odd-order terms from the previous relation are usually cancel out, so the main circuit nonlinearity caused by the second-order effects will be represented by the third-order error term from the previous relation, having much smaller value than the linear term.

2.5. The current-pass circuit

The necessity of designing this circuit is derived from the requirement that the same current to pass between the two output pins, X and Y. The implementation in CMOS technology of this circuit is very simple, consisting in a simple and a multiple current mirrors (Figure 3).

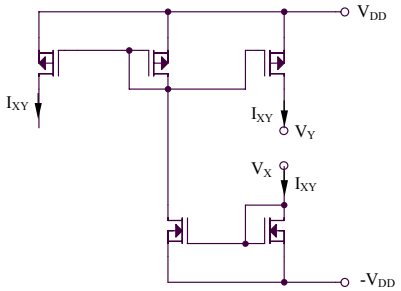

Figure 3: The current-pass circuit

2.6. The multiplier circuit

The original idea for obtaining the multiplying function is to use two identical square-root circuits, implementing the following functions:

$$I_{OUT1} = 2\sqrt{I_O I_2} \tag{14}$$

and:

$$I_{OUT2} = 2\sqrt{I_{XY} I_1}. \tag{15}$$

I_{OUT1} and I_{OUT2} being the output currents of these square-root circuits. Using a classical current mirror, it is possible to impose that $I_{OUT1} = I_{OUT2}$, resulting the necessary multiplying function:

$$I_{XY} = I_O \frac{I_2}{I_1}. \tag{16}$$

The important advantages of this implementation are represented by the increased frequency response that could be obtained as a result of the current-mode operation of the multiplier circuit and of the biasing in saturation of all the MOS active devices and, additionally, by the reduced

silicon occupied area achieved by using exclusively MOS transistors.

2.7. Active resistor with negative equivalent resistance

Active resistors with controllable negative equivalent resistance cover a specific area of VLSI designs, finding very large domains of applications such as the canceling of an operational amplifier load or the design of integrators with improved performances. In order to obtain a negative equivalent active resistance circuit, the block diagram from Figure 1 must be modified by inversing the sense of the I_{XY} current passing through the I block, resulting an equivalent resistance expressed by:

$$R_{ech.}' = -\frac{V_0}{I_0}\sqrt{\frac{(W/L)_1}{(W/L)_2}\frac{I_{01}}{I_{02}}} \quad . \tag{17}$$

III. CONCLUSIONS

A new active resistor circuit has been presented. The main advantages of the original proposed implementation are the improved linearity, the small area consumption and the improved frequency response. An original technique for linearizing the $I(V)$ characteristic of the active resistor has been proposed, based on the simulation of the Ohm law using two linearized differential amplifiers, a multiplier and a current-pass circuit. The controllability of the active resistor circuit is excellent, existing the possibility of modifying the value of the equivalent resistance by changing the ratio between a control voltage and a control current. Additionally, the value of the simulated resistance is not function on technological parameters, with the result of an improved circuit accuracy. The errors introduced by the second-order effects have been also strongly reduced, while the area consumption of the active resistor has been minimized by replacing the classical MOS transistor with FGMOS devices. As a result of the proposed linearization technique designed for the differential amplifier from Figure 2, the linearity (9) of its transfer characteristic is referring both to small and large signal operation, being limited only by the second-order effects that affect the MOS transistors' operation. The consequence will be a relatively large range of the input voltage that could be applied across the input pins (V_X and V_Y from Figure 1), respecting the important restriction of maintaining the estimated circuit linearity.

ACKNOWLEDGMENTS

The work has been co-funded by the Sectoral Operational Programme Human Resources Development 2007-2013 of the Romanian Ministry of Labour, Family and Social Protection through the Financial Agreement, POSDRU/89/1.5/S/62557.

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