QUADRATIC COMPUTATIONAL CIRCUITS FOR VLSI DESIGNS

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ABSTRACT

There will be presented two important classes of computational circuits, implementing squaring and square-rooting functions. Representing a basis for obtaining all the continuous functions, the previous mentioned functions will be implemented using MOS active devices biased in the saturation region, having the advantage of an important increasing of the circuits' frequency response. For the same reason, a current-mode operation of the circuits will be imposed, the increasing of the computing speed being associated with the independence of the circuits' performance on the technological parameters. Additionally, the VLSI implementation assures a theoretically important speed increasing of the designed circuits.

The circuits' complexity will be strongly reduced by replacing classical MOS transistors by FGMOSTs (Floating Gate MOS Transistors), while the proposed design techniques assure a relatively small dependence of the circuits' performances on the second-order effects that affect the MOS transistor operation.

Keywords: computational circuits, current-mode operation, VLSI design

1. INTRODUCTION

Computational circuits are important building blocks in telecommunications or medical equipments, finding also many applications in analog signal processing because of an important decreasing of the computational time for the VLSI implementations of mathematical functions with respect to other possible approaches. Additionally, an important reduction of the circuits' complexity and an improvement of their possibility of integration could be obtained by choosing the VLSI implementation. Due to the rapid development of CMOS VLSI technology, many analog signal-processing functions can be achieved by employing the square-law model of MOS transistors working in saturation. Based on this principle, several basic building blocks, such as multipliers, active resistors and transconductors have been developed.

The squaring and square-rooting functions represent very important functions that could be obtained in CMOS technology, representing a basis for implementing all the other continuous functions by using a polynomial series expansion. It is obvious the necessity of making a compromise between the circuit complexity and the approximation error.

There are many possibilities [1]-[5] of implementation squaring and square-rooting circuits using the quadratic characteristic of the MOS transistor in saturation. The main goals of this class of circuits are the silicon occupied area, the independence of the output current on the technological parameters (associated with an independence on temperature of circuit performances) and a small sensitivity to the second-order effects (bulk effect, channel length modulation and mobility degradation).

2. THE VLSI IMPLEMENTATION OF CURRENT-MODE SQUARER CIRCUITS

2.1. The first CMOS current squarer

The original implementation of a CMOS current squarer using a FGMOS transistor is presented in Figure 1.

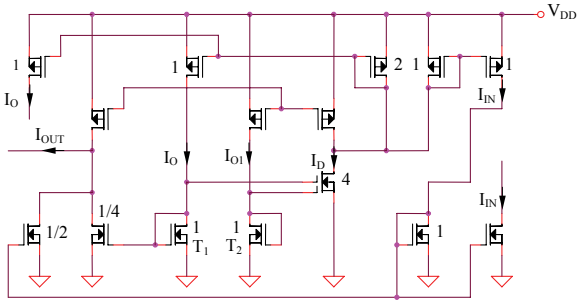

Figure 1: CMOS squarer using a FGMOS transistor

The FGMOS transistor is a MOS transistor whose gate is floating, being capacitive coupled to the multiple input gates. The drain current of a FGMOS transistor with n-input gates working in the saturation region is given by the following equation:

$$I_D = \frac{K}{2}\left[\sum_{i=1}^{n} k_i\left(V_i - V_S\right) - V_T\right]^2, \qquad (1)$$

where $K = \mu_n C_{ox}(W/L)$ is the transconductance parameter of the transistor, μ_n is the electron mobility, C_{ox} is the gate oxide capacitance, W/L is the transistor

aspect ratio, $k_i, i = 1,...,n$ are the capacitive coupling ratios, V_i is the i-th input voltage, V_S is the source voltage and V_T is the threshold voltage of the transistor. Considering that all MOS transistors from Figure 1 are working in saturation and $k_1 = k_2 = 1/2$, the expression of the drain current of the FGMOS transistor could be written as:

$$I_D = \frac{4K}{2}\left(\frac{1}{2}V_{GS_1} + \frac{1}{2}V_{GS_2} - V_T\right)^2, \quad (2)$$

where V_{GS_1} and V_{GS_2} represents the gate-source voltages of T_1 and T_2 transistors, respectively. It results the following dependence of the FGMOS transistor drain current on I_O and I_{O_1} currents:

$$I_D = I_O + I_{O_1} + 2\sqrt{I_O I_{O_1}}, \quad (3)$$

equivalent with:

$$I_{O_1} = \frac{(I_O + I_{IN})^2}{4I_O} = \frac{I_O}{4} + \frac{I_{IN}}{2} + \frac{I_{IN}^2}{4I_O}. \quad (4)$$

Thus, the output current expression is $I_{OUT} = I_{IN}^2 / 4I_O$. The most important advantage of the original implementation of the current squarer proposed in Figure 1 is the absolutely (in a first-order analysis) independence of the output current on technological parameters (K, V_T).

2.2. The second CMOS current squarer

Another original idea for implementing the current-mode squarer is to use two groups of cascaded MOS transistors, the devices from the first group being biased at the same drain current, while each MOS transistor from the second group works at different drain currents.

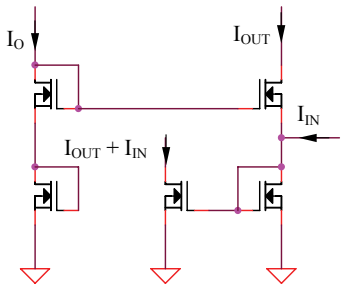

Figure 2: The current-mode CMOS squarer

Considering a strong inversion (saturation) operation of all MOS transistors from Figure 2, it is possible to write that:

$$2\sqrt{I_O} = \sqrt{I_{OUT}} + \sqrt{I_{OUT} + I_{IN}}, \quad (5)$$

resulting:

$$I_{OUT} = I_O - \frac{I_{IN}}{2} + \frac{I_{IN}^2}{16I_O}. \quad (6)$$

Subtracting I_O current and adding $I_{IN}/2$ current to the previous relation of I_{OUT}, it is possible to obtain an output current proportional to the square of the input current.

2.3. The third CMOS current squarer

The third circuit of the current squarer is presented in Figure 3.

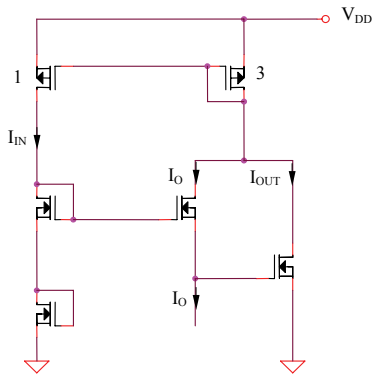

Figure 3: The circuit for implementation squaring function

Considering that all transistors from Figure 3 are working in saturation, it is possible to write:

$$2\sqrt{I_{IN}} = \sqrt{I_O} + \sqrt{I_{OUT}}. \quad (7)$$

Because of the PMOS current mirror having a current ratio equal to 3 it results $I_O + I_{OUT} = 3I_{IN}$. Thus, the output current of the circuit presented in the previous figure will be proportional to the square of the input current I_{IN}, $I_{OUT} = I_{IN}^2 / 4I_O$.

3. THE VLSI IMPLEMENTATION OF CURRENT-MODE SQUARE-ROOT CIRCUITS

3.1. The first square-root circuit

The new proposed implementation of the square-root circuit is based on a structure similar to the current squarer from Figure 1. The square-root circuit using MOS transistors working in saturation and a FGMOS transistor for reducing the circuit complexity is presented in Figure 4.

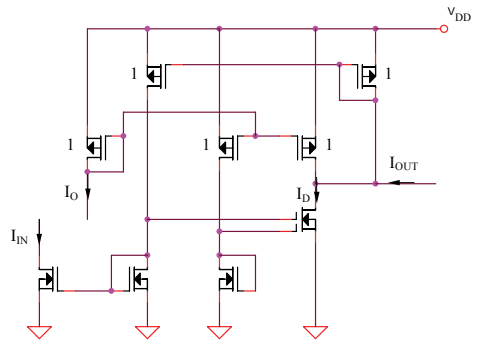

Figure 4: Square-root circuit using a FGMOS transistor

The expression of the drain current for the FGMOST from Figure 4 is:

$$I_D = I_O + I_{IN} + 2\sqrt{I_O I_{IN}} \,. \tag{8}$$

Because of the PMOS current mirrors it is possible to write $I_D = I_O + I_{IN} + I_{OUT}$, resulting the following expression of the output current:

$$I_{OUT} = 2\sqrt{I_O I_{IN}} \,. \tag{9}$$

3.2. The second square-root circuit

Considering an operation in saturation of all MOS transistors, the current I_D will have the following expression:

$$I_D = I_O - \frac{I_{OUT}}{2} + \frac{I_{OUT}^2}{16 I_O} \,. \tag{10}$$

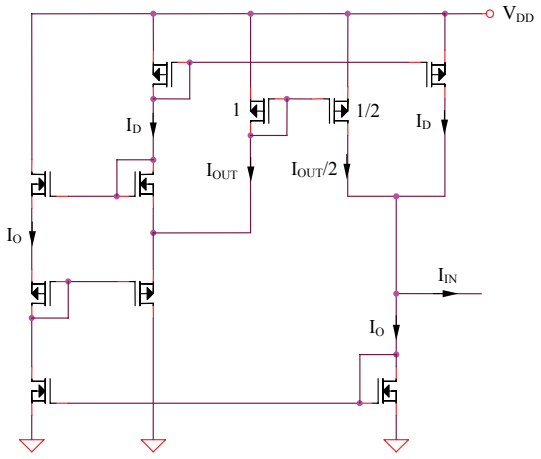

Figure 5: The square-root circuit

Because $I_D + I_{OUT}/2 = I_{IN} + I_O$, it results:

$$I_{OUT} = 4\sqrt{I_O I_{IN}} \,. \tag{11}$$

3.3. The third square-root circuit

The core of the square-root circuit is derived from the current squarer presented in Figure 2.

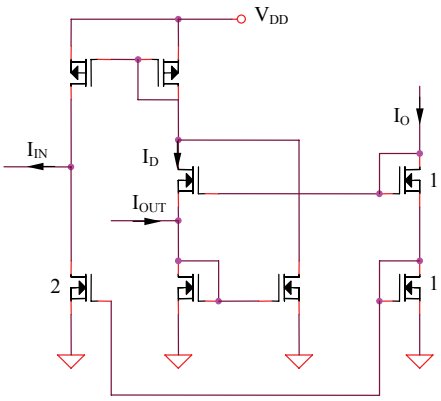

Figure 6: The current-mode square-root circuit

Similarly to the current squarer, it is possible to write that:

$$2\sqrt{I_O} = \sqrt{I_D} + \sqrt{I_D + I_{OUT}} \,, \tag{12}$$

resulting:

$$I_D = I_O - \frac{I_{OUT}}{2} + \frac{I_{OUT}^2}{16 I_O} \tag{13}$$

and:

$$2\left(I_O - \frac{I_{OUT}}{2} + \frac{I_{OUT}^2}{16 I_O}\right) + I_{OUT} - 2I_O = I_{IN} \,. \tag{14}$$

So, the output current I_{OUT} will be proportional with the square-root of the input current I_{IN}:

$$I_{OUT} = \sqrt{8 I_O I_{IN}} \,. \tag{15}$$

4. CONCLUSIONS

There were presented two important classes of computational circuits, implementing squaring and square-rooting functions. Representing a basis for obtaining all the continuous functions by expanding them in Taylor series, the previous mentioned functions have been implemented using exclusively MOS active devices biased in the saturation region, having the important advantage of an important increasing of the circuits' frequency response. For the same reason, a current-mode operation of the circuits has been imposed, the increasing of the computing speed being associated to the independence of the circuits' performance on the technological parameters. Additionally, the VLSI implementation of the computed functions assures a theoretically important speed increasing of the designed circuits.

The circuits' complexity has been strongly reduced by replacing classical MOS transistors by FGMOSTs (Floating Gate MOS Transistors), while the proposed design techniques assure a relatively good independence of the circuits' performances on the second-order effects that affect the MOS transistor operation.

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