

# A NEURAL MAXIMUM SELECTOR: EXPLICIT PARAMETER SET-UP FOR TIME PERFORMANCE

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## ABSTRACT

A continuous time neural network of Hopfield type is considered. It is a W(inner) T(akes) A(ll) selector. Its inputs are capacitively coupled to model the parasitics or faults of overcrowded chip layers. A certain parameter setting allows the correct selection of the maximum element from an input list. As processing time is a performance criterium, we infer upper bounds of it, explicitly depending on circuit and list parameters. Our method consists of converting the system of nonlinear differential equations describing the circuit to a system of decoupled linear inequalities.

Keywords: neural networks, winner-takes-all, Hopfield networks, parasitics, time evaluations.

## 1. INTRODUCTION

We consider a neural network of  $N$  cells with a complete interconnection of negative feedback type. We design it as a WTA machine, i.e. a mean of separating the largest signal from a list of constant and distinct signals. This is an up to date topic in time problems for neural networks of analog type (Wu 2001, Cao 2001, Zhang, Heng and Fu, 1999; Liang and Si 2001, Cho 2005). It follows the pioneering papers regarding the computational Hopfield networks (Hopfield 1984, Hopfield and Tank 1985, Majani, Erlanson and Abu-Mostafa 1989; Atkins 1992, Dranger and Priemer 1997).

Referring to Fig. 1 each cell is an ideal amplifier with  $v_i = mg(\lambda u_i)$  where  $g$  is a “sigmoid” i.e.  $g : \mathcal{R} \rightarrow (-1,1)$ ,  $g'(x) \geq a > 0$ ,  $\lim_{x \rightarrow \pm\infty} g(x) = \pm 1$  and  $\lim_{x \rightarrow \pm\infty} xg'(x) = 0$ .  $\lambda > 0$  is “the gain”. Apart from interconnections  $p > 0$  we consider here the mutual capacitance  $\delta$  between all pairs of inputs. It models the unavoidable parasitic effects on the crowded chips. We are interested in the influence of these capacitances on the network performances: is the WTA

selection still working? How much is the network speed affected?

The processing list is fed by current sources  $d_i$  ordered as:

$$d_{\sigma(1)} > d_{\sigma(2)} > \dots > d_{\sigma(N)} \quad (1)$$

where  $\sigma(i)$  is a permutation of indices 1 to  $N$ . The network should signal that  $d_{\sigma(1)}$  is the “winner”. This is done by choosing proper values of circuit parameters  $M$ ,  $\lambda$ ,  $m$ ,  $a$ ,  $p$ ,  $l$  including the  $[0, d_{\max}]$  admission interval and  $t_p$ , the clocking time. Also we have to take into account the minimum density  $z$  of arriving sequence of lists, which is  $z = \frac{\Delta(N-1)}{d_{\max}}$

where  $\Delta = \min |d_i - d_j|$ .

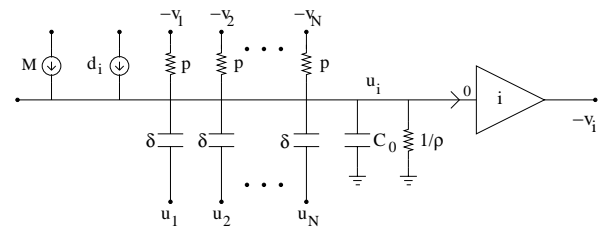


Figure. 1: The  $i$ -th cell with all its interconnections

The network in Fig. 1 is described by

$$C \frac{du}{dt} = -lu - Tv + b \quad (2)$$

where  $u = (u_1, \dots, u_N)^{tr}$ ,  $v = (v_1, \dots, v_N)^{tr}$ ,  $b = (b_1, \dots, b_N)^{tr}$  with  $b_i = d_i + M$ .  $C$  is the capacitance matrix with  $C_{ii} = C_0 + (N-1)\delta$  and

$C_{ij} = -\delta$ .  $T$  is the resistive interconnection matrix,  
 $T_{ii} = 0$ ,  $T_{ij} = p > 0$ . Also  $l = \frac{1}{\rho} + (N-1)p$ .

As we show elsewhere, for each initial condition (2) has a unique solution  $u(t)$  defined on  $[0, \infty)$ . Also, for almost all vector sources  $b \in \mathfrak{R}^N$  (2) has a finite number of equilibria  $\bar{u}$ . They are solutions of the stationary equation

$$0 = -lu - Tv + b \quad (3)$$

We can also show that the old Liapunov function introduced by Hopfield (Hopfield 1984), namely

$$E(u) = \frac{1}{2} \langle Tv, v \rangle - \langle b, v \rangle + \frac{l}{m\lambda} \sum_{i=1}^N \int_0^{v_i} g^{-1} \left( \frac{x}{m} \right) dx$$

works for our special case of  $C$  being non-diagonal. This implies that for any solution  $u(t)$  of (2) there exists an equilibrium  $\bar{u}$ , solution of (3), such that  $u(t) \rightarrow \bar{u}$  when  $t \rightarrow \infty$ .

The proofs are omitted below. They can be found by the methods in (Calvert and Marinov 2000, Marinov and Calvert 2003, Marinov and Hopfield 2005, Chen, Lu and Amari 2002; Costea 2007, Costea and Marinov 2006, Costea and Marinov 2007).

## 2. THE WTA SELECTOR

Here we give conditions on circuit and list parameters such that once the list (1) arrives, the circuit evolves toward an equilibrium  $\bar{u}$  with

$$\bar{u}_{\sigma(1)} > \beta > -\beta > \bar{u}_{\sigma(i)} \quad (4)$$

for all  $i \in \overline{2, N}$ . Here  $\beta$  is a threshold assuring a convenient resolution of output.

The first result we give is “the ordering” property of the dynamic solution. This is, starting from zero and imposing  $\lambda > \frac{l}{pam}$  the order in (1) (where we took

$\sigma(i) = i$  for writing simplicity) transfers to  $u(t)$ :

$$u_1(t) > u_2(t) > \dots > u_N(t) \quad (5)$$

for all  $t > 0$ . Then, by using “the difference equation”

$$0 = -l(\bar{u}_i - \bar{u}_{i+1}) + p(\bar{v}_i - \bar{v}_{i+1}) + d_i - d_{i+1} \quad (6)$$

and the above convergence, we derive

$$\bar{u}_1 > \bar{u}_2 > \dots > \bar{u}_N \quad (7)$$

Next, we can show the WTA property

$$\bar{u}_1 > \beta > -\beta > \bar{u}_2 > \bar{u}_3 > \dots > \bar{u}_N \quad (8)$$

provided that the following conditions are met:

$$\Delta \geq 2l\beta \quad (9)$$

$$M \geq l\beta - p(N-1)\xi - \underline{d}_1 \quad (10)$$

$$M \leq -l\beta + p\xi - p(N-2)m - \bar{d}_2 \quad (11)$$

Here  $\xi = mg(\lambda\beta)$ ,  $\underline{d}_1 = zd_{\max}$  is the lowest  $d_1$  and  $\bar{d}_2 = d_{\max} - (N-2)\Delta$  is the highest  $d_2$ . Thus (9)-(11) give conditions for (8) regardless the lists with density bigger than  $z$ .

## 3. TIME BOUNDS

We try now to obtain a clocking time for our machine. The moment  $t_p$  when we should stop the transient of  $u(t)$  towards  $\bar{u}$  is when the WTA property (8) of  $\bar{u}$  is fulfilled:

$$u_1(t_p) > \beta > -\beta > u_2(t_p) > \dots > u_N(t_p) \quad (12)$$

As  $t_p$  is unknown, we try to obtain an upper bound of it  $T_p$  at which (12) is still valid.

We distinguish two cases – Figs 2 and 3.

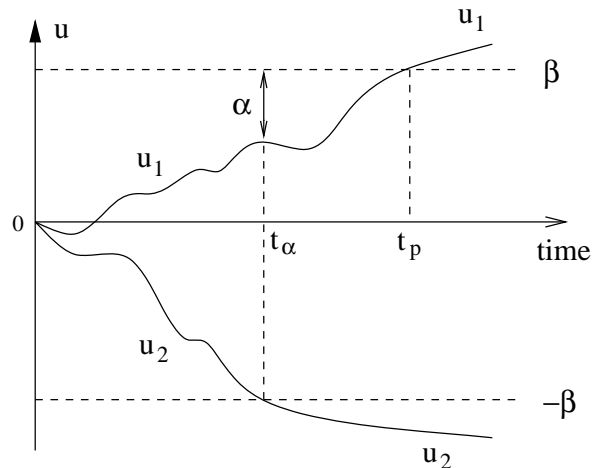


Figure. 2 The processing phase - case 1. The  $u_{\sigma(1)}$  winner surpasses the threshold  $\beta$  after the moment when the losers  $u_{\sigma(2)}$  fall under  $-\beta$

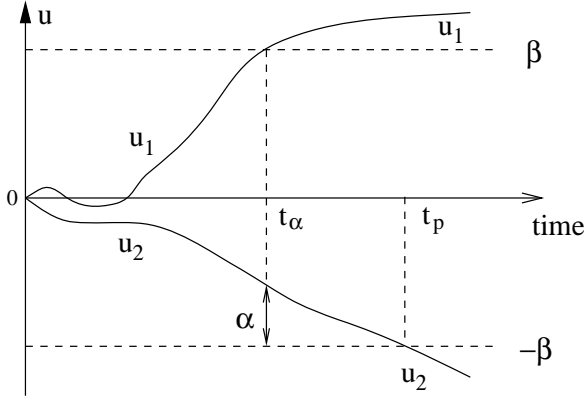


Figure. 3 The processing phase - case2. The  $u_{\sigma(1)}$  winner goes above  $\beta$  before the moment when  $-\beta = u_{\sigma(2)}$ .

The first one, supposes  $u_2(t)$  passes the WTA threshold  $-\beta$  before  $u_1(t)$  crosses its  $+\beta$  level. Rigorously speaking, we suppose  $\alpha \in [0, 2\beta]$  and take the moment  $t_\alpha$  when  $u_1(t_\alpha) = \beta - \alpha$ ,  $u_2(t_\alpha) = -\beta$  and for all  $t > t_\alpha$ ,  $u_2(t) < -\beta$ . The second case supposes  $u_1(t)$  reaches  $+\beta$  in advance of  $u_2(t)$  touching  $-\beta$ . In this case we call  $t_\alpha$  the moment when  $u_1(t_\alpha) = \beta$ ,  $u_2(t_\alpha) = -\beta + \alpha$  and for all  $t > t_\alpha$   $u_1(t) > \beta$ . In both cases above we call  $t_p$  -processing time-, the first moment after  $t_\alpha$  when  $u_1(t_p) \geq \beta$  and  $u_2(t_p) \leq -\beta$ . With these, the problem of finding the clocking time  $T_p$  reduces to search for upper bounds  $\bar{t}_\alpha$  and  $\overline{t_p - t_\alpha}$  of  $t_\alpha$  and  $t_p - t_\alpha$  respectively. We have  $T_p(\alpha) = \bar{t}_\alpha + \overline{t_p - t_\alpha}$ . The first bound  $\bar{t}_\alpha$  comes from “the difference equation”

$$C_n \frac{d}{dt}(u_1 - u_2) = -l(u_1 - u_2) + p(v_1 - v_2) + d_1 - d_2$$

where  $C_n = C_0 + N\delta$ . With  $(u_1 - u_2)(0) = 0$  and  $(u_1 - u_2)(t_\alpha) = 2\beta - \alpha$  we get

$$t_\alpha \leq \bar{t}_\alpha = \frac{C_n}{l} \ln \frac{\Delta}{\Delta - l(2\beta - \alpha)} \quad (13)$$

This is valid equally for the two cases and all  $\alpha \in [0, 2\beta]$ .

The evaluation of  $t_p - t_\alpha$  in case 1 comes from the first equation in (2) written as:

$$C_0 \frac{du_1}{dt} = -lu_1 - \delta \sum_{j=1}^N \frac{d}{dt}(u_1 - u_j) - p \sum_{j=2}^N v_j + b_1$$

It yields

$$t_p - t_\alpha \leq \overline{t_p - t_\alpha} = \frac{C_0}{l} \ln \frac{W - l\beta + l\alpha}{W - l\beta} \quad (14)$$

where

$$W = p\xi(N-1) + \underline{d}_1 + M - \frac{\delta}{C_n} [2pm(N-1) + \sum_{j=1}^N \bar{d}_{1j}] \quad (15)$$

Here  $\underline{d}_1 = zd_m$  and  $\bar{d}_{ij} = d_m - (N-j)\Delta$ .

For the case 2 we use the second equation in (2)

$$C_0 \frac{du_2}{dt} = -lu_2 - \delta \sum_{j=1}^N \frac{d}{dt}(u_2 - u_j) - p \sum_{\substack{j=1 \\ j \neq 2}}^N v_j + b_2$$

and get again (14) where

$$W = p\xi - pm(N-2) - \bar{d}_2 - M - \frac{\delta}{C_n} [2pm(N-1) + \bar{d}_{12}] \quad (16)$$

Here  $\bar{d}_2 = d_m - \Delta$  and  $\bar{d}_{12} = d_m - (N-2)\Delta$ .

Now, (13) and (14) give the bound  $T_p(\alpha)$  of processing time for every  $\alpha \in [0, 2\beta]$ . By imposing  $\frac{dT_p}{d\alpha} < 0$  we find  $\max T_p(\alpha) = T_p(0)$  which gives a final bound:

$$t_p \leq T_p(0) = \frac{C_n}{l} \ln \frac{\Delta}{\Delta - 2l\beta} \quad (17)$$

The above imposition results in

$$W - l\beta > 0 \quad (18)$$

for both two cases, and also  $\Delta - 2l\beta > 0$  as in (9). These inequalities are made true by a proper choosing of circuit parameters  $M$ ,  $\xi$ ,  $\beta$ ,  $m$ ,  $p$ ,  $d_m$  when

the minimum list density  $z$  and the maximum parasitic capacitance  $\delta$  are given. Our evaluations works for  $\delta \in [0, C_0/N - 2]$ .

Also, in this context we can answer the natural question: “is the processing time longer when the parasitic capacitance increases?” For these, by knowing from above that the maximum of  $t_p$  happens when  $u_1$  and  $u_2$  simultaneously reach  $+\beta$  respectively  $-\beta$ , we give bilateral bounds of  $t_p$ :

$$\frac{2p\xi + d_{12}}{2p\xi + d_{12} - 2l\beta} \leq e^{\frac{l}{C_n}t_p} \leq \frac{d_{12}}{d_{12} - 2l\beta} \quad (19)$$

If  $t_p^\delta$  is the processing time with parasitic capacitance  $\delta$  then the from (19) we can easily infer  $t_p^\delta \geq t_p^{\delta=0}$  for

$$\delta > \frac{2pm}{N(\Delta - 2l\beta)} C_0.$$

#### 4. CONCLUSION

All of above give analytical relations between parameters to fulfill the WTA property. They are (9)-(11) and (18). The clocking time is given by (17), which provides a mean to influence the processing speed when the crosstalk is considered and very tight lists are fed. The assumptions under which our results are reasonable for practical purposes.

#### REFERENCES

- Wu, J., 2001 *Introduction to neural dynamics and signal transmission Delay*, Berlin, NY, Walter de Gruyter,.
- Gupta M.M., Jin L. and Homma N., 2003, *Static and Dynamic Neural Networks from Fundamentals to Advanced Theory*, Hoboken, IEEE Press, Wiley-Interscience.
- Hopfield J.J., 1984, Neurons with graded response have collective computational properties like those of two state neurons, *Proc. Nat. Academy Sci.*, Vol. 81, pp. 3088-3092.
- Hopfield J.J. and Tank D. W., 1985, Neural computation of decisions optimization problems, *Biol. Cybern.*, vol. 52, pp. 141-152.
- Atkins M., 1992, Sorting by Hopfield nets, *Proc. Int. Joint Conf. Neural Networks*, vol. 2, pp. 65-68, Washington DC.
- Dranger T.S. and Priemer R., 1997 Collective process circuit that sorts, *IEE Proceedings-Circuits, Devices, Syst.*, vol. 144, pp. 145-148.
- Cao J., 2001, Global exponential stability of Hopfield neural networks, *Int. J. Syst. Sci.*, Vol. 32, no. 2, pp. 233-236.

- Majani E., Erlanson R. and Abu-Mostafa Y., 1989, On the K-winner-take-all network, *Advances in Neural Information Processing Systems*, D.S. Touretzky, Ed. San Mateo, CA: Morgan-Kafmann, vol.1, pp. 634-642.
- Zhang Y., Heng P.A. and Fu W. C., 1999, Estimate of exponential convergence rate and exponential stability for neural network, *IEEE Trans. Neural Networks*, vol. 10, no. 6, pp. 1487-1493.
- Liang X. and Si J., 2001, Global exponential stability of neural networks with globally Lipschitz continuous activations and its application to linear variational inequality problem, *IEEE Trans. on Neural Networks*, Vol. 12(2), pp. 349-359.
- Chen T., Lu W. and Amari S., 2002, Global Convergence Rate of Recurrently Connected Neural Networks, *Neural Computation*, vol. 14, pp. 2947-2957.
- Calvert B. and Marinov C. A., 2000, Another K-winners-take-all analog neural network, *IEEE Trans. Neural Networks*, Vol.11, pp. 829-838.
- Marinov C. A. and Calvert B. D., 2003, Performance analysis for a K-Winners-Take-All analog neural network: Basic theory, *IEEE Trans. Neural Networks*, Vol. 14, pp. 766-780.
- Cho K., 2005, Delay calculation capturing crosstalk effects due to coupling capacitors, *Electronic Letters*, Vol. 41, no. 8, pp. 458-460.
- Marinov C. A. and Hopfield J. J., 2005, Stable computational dynamics for a class of circuits with  $O(N)$  interconnections capable of KWTA and rank extractions, *IEEE Trans. Circuits and Systems, Part I*, Vol. 52, pp. 949-959.
- Costea R. L., 2007, *Artificial neural systems - Switching times for WTA circuits of Hopfield type*, Doctoral Disertation, Polytechnic University of Bucharest.
- Costea R. L and Marinov C.A., 2006, Capacitive cross-coupling faults and WTA correct behaviour, *Proc of 10<sup>th</sup> IEEE Workshop on Signal Propagation on Interconnects*, pp. 189-192, Berlin, Germany.
- Costea R. L and Marinov C.A., 2007, Clocking and WTA design of a continuous time Hopfield net with parasitic capacitances, *European Conference on Circuit Theory and Design*, Seville, Spain.

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