MODELING AND SIMULATION OF A NANOSTRUCTURE FOR A SINGLE ELECTRON TECHNOLOGY IMPLEMENTATION

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ABSTRACT
The Electronic Devices Simulators are valuable tools used in micro and nano-electronics labs. This paper analyses the electrical characteristics evolution, under the down-scaling sizes tendency of the SOI devices. A nanostructure sub-10nm Si film thickness with a vacuum cavity in the device body was simulated. The global current is a superposition of a tunnel current through the cavity and an inversion current at the film bottom. The tunnel source-drain current prevails in devices with sub 10nm film thickness and provides the I_D-V_{DS} characteristics with a minimum. For film thickness comprised between 200-10nm, the I_D-V_{GS} curves preserve similar shapes with a classical MOS/ SOI's transfer characteristics. For sub 10nm film thickness, the shape of the I_D-V_{GS} characteristics tends to have a maximum, like in Single Electron Device SED.

Keywords: Few Electrons Transistors, SOI structures, simulations of nano-devices.

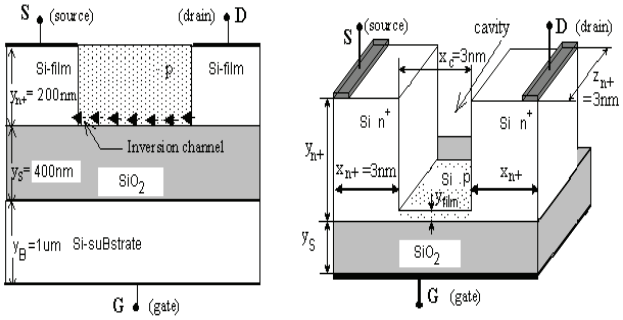
1. INTRODUCTION

The approach of the nowadays micro and nano-electronics themes, at laboratory level in a university without a technological park, is possible just with strong simulators.

In this paper, the some virtual measurements of the SOI transistors with nano-metric films thicknesses are presented. The reference device was a standard SOI-MOSFET, 200nm Si-film on 400nm Oxide (Ravariu and Rusu 2006), fig.1.a. The I_D (V_{DS}, V_{GS}) curves were studied for thinner films: 10nm, 1nm, 0.3nm. For sub-10nm film thickness, a new structure with a nano-cavity, was proposed in fig.1.b. The source and drain regions consist in two high "undulations" of Si-n^+ (y_{n+}=7nm) onto an oxide support. The Si-p transistor body was thinned firstly to y_{film}=1nm and secondly to y_{film}=0.3nm. The carriers transport was confined at the limit, one by one. Essentially, the device could be regarded as a string of "Few Electron Transistors" that converges to the "Single Electron Transistor" (SET), as an ideal limit. Another reason for two prominent n^+ - undulations is related to the practical possibility of Source and Drain metallization. On the other hand, both thick parallelepiped n^+ - layers fulfill the electron reservoir role, like in a SET, (Mahapatra, Ionescu, and Banerjee 2002).

2. THE NOVEL DEVICES ARCHITECURE

The device architecture, presented in fig.1.b, was inspired from a real sub-10nm undulated polysilicon film, (Badila, Ecoffey, Bouvet, and Ionescu 2003). Secco etching in $K_2Cr_2O_7$:HF solution, which currently is applied for the crystalline defects revealing in silicon, preferentially etches the boundaries of the poly-silicon grains, producing undulated poly-silicon layer with maximum 6 nm and minimum 3 nm thickness. The thin undulated poly-silicon films are deposited onto an insulator material. The electrical stimulus were in the range: -3 ÷ +3V, -10V ÷ +10V, -15V ÷ +15V, (Eccofey, Bouvet, Fazan, Tringe, and Ionescu 2003).



(a) (b)

Figure 1: (a) The current flow in a cross-section of a 200nm SOIMOSFET; (b) the nanotransistor with a cavity

Starting from these experimental data, we developed a new device configuration with the source and drain regions are n^+-type silicon (N_D=10^{17}cm^{-3}) with x_{n+}=3nm, y_{n+}=7nm, z_{n+}=6nm, placed at x_c =3nm distance. A thinner p – type Si film (N_A=$5\cdot10^{15}$cm^{-3}) links the source and drain regions and represents the inversion channel location. All these parameters will be

maintained constant during the simulations. Thinning the p-type film to y_{film}=1nm, a cavity carried out between source and drain.

3. THE ANALYTICAL MODEL

For small vacuum distance d, the source-drain tunneling probability is described by the Fowler-Nordheim model, (Rusu, 2000):

$$P_t \approx exp\left[-\frac{4\sqrt{2m_n^*}\cdot\chi_S^{3/2}\cdot d}{3q\hbar V_{DS}}\right]. \quad (1)$$

where m_n^* is the electron effective mass, χ_S is the semiconductor affinity for electrons in respect with the vacuum, $\hbar=h/2\pi$ (h is the Planck's constant), q is the elementary electric charge.

The tunnel effect through a triangle potential barrier is the main phenomenon in the proposed SOI transistor with a cavity. Some electrons tunnel the Si - Vacuum barrier, producing the tunnel current, I_t , (Rusu, 2000):

$$I_t = \frac{A}{\sqrt{E_b}}\cdot\left(\frac{V_{DS}}{x_c}\right)^2\cdot\exp\left(\frac{B\cdot E_b^{3/2}\cdot x_c}{V_{DS}}\right). \quad (2)$$

where $E_b = \chi_{semic} - \chi_{vacuum}$ is the height of the triangle barrier of the potential from semiconductor to vacuum and A, B are some material parameters depending on the effectiveness mass for electrons and holes.

Considering x_C as constant parameter, the variation of the tunnel current I_t, versus the drain-source voltage V_{DS} is analytically studied via the first order derivative. Because the function $I_t'(V_{DS})$ is positive for $V_{DS}>0$, the tunnel current monotonically increases with the drain-source voltage.

Zeroing the first order derivative of the model (1) results a minimum for the tunnel current versus V_{DS} voltage:

$$V_{DS}\big|_{I_t=\min} = \frac{B\cdot E_b^{3/2}\cdot x_c}{2}. \quad (3)$$

The simulations proved that the total current preserve the curvature with a minimum when the film thickness decreased under 1nm because the percentage of the tunnel current, I_t overcomes that from the inversion channel, I_{MOS}. For thicker Si-p film (y_{film}>10nm), the tunnel current is negligible and the characteristics tends to those of the classical SOI-MOSFET. The cavity itself has a high vacuum. The number of air molecules N, in the cavity volume for y_{film}=1nm, is:

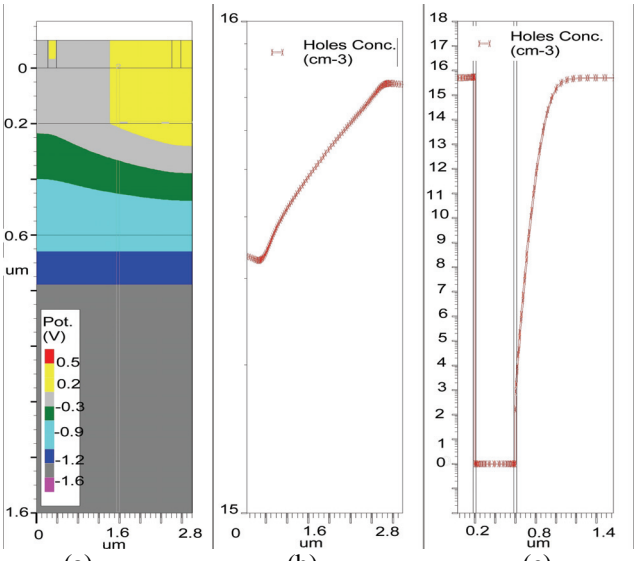
$$N = \frac{x_c\cdot(y_{n+}-y_{film})\cdot z_{n+}\cdot N_{A0}}{V_{m0}}. \quad (4)$$

That means N ≈ 2 air molecules. Hence, the electrons will not be disturbed by the air molecules from cavity, in normal conditions (N_{A0} = 6,023×10^{23} molecules/mol, V_{m0} = 22,42 dm^3/mol). Consequently, the device manufacturing doesn't require a special vacuum technology.

4. THE SIMULATION RESULTS FOR THE SOI STRUCTURE WITHOUT CAVITY

In the ATLAS simulations, the constructive data of the nanotransistor were: y_{n+}=0.2µm, y_S=0.4µm and y_B=1µm, the doping concentrations in film and substrate N_A=2×10^{15}cm^{-3}. The applied voltages were V_G= 0V… -3V, V_D=0V… +4V, V_S=0V.

Figure 2.a presents the potential distribution and the holes concentration in an intermediate situation at V_G = -1,8V, through the structure with 200nm Si-film thickness. A negative gate bias induces a holes crowding in the p-type film. Near drain, where V_{GD} is higher than V_{GS}, the holes reached p=8x10^{15}cm^{-3} and near source p=4x10^{15}cm^{-3} > 2x10^{15}cm^{-3} = N_A, fig.2.b. From the longitudinal holes distribution can be observed the holes concentration decreasing in the substrate, fig.2.c. This simulation proves the substrate depletion effect.



(a) (b) (c)

Figure 2: (a) The potential distribution in the 200nm SOI structure; (b) the holes concentration accros the structure; (c) the holes concentration along the structure

Figure 3 presents the electron concentration in the structure with 200nm film thickness. A positive gate bias induces an electron inversion channel in p-type film (e.g. $n\big|_{y=0.2um} = 10^{16}\,cm^{-3} > 5\cdot10^{15}$cm^{-3}=$N_{A\text{-}film}$), figure 3.

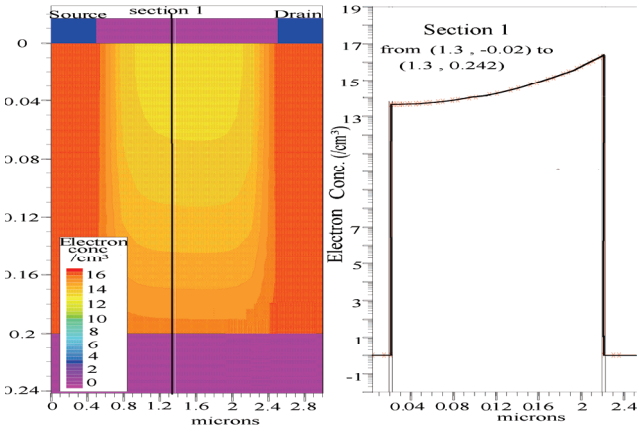


Figure 3: Detail in film for the electron concentration

5. THE SIMULATION RESULTS FOR THE SOI STRUCTURE WITH A NANO-CAVITY

In the simulations, the constructive data were those described in the paragraph 2.

The main physical effects were included as "nano-effects": Band to Band Tunnelling, Fowler-Nordheim tunnelling, Fermi distribution, including in the MODEL statement the following parameters: BBT, FNORD, FERMI. Figure 4 presents the total current vectors in 1 nm-film at V_{DS}=4V, V_{GS}=3V, besides to the electrons concentration in the channel region. The vectors through the vacuum (emphasised by black line), proved the tunnel effect. A value about $10^{20}cm^{-3}$ means 1 electron/channel, which shows our target: Single Electron Working regime for nanostructure, fig.5.

In fig. 6.a a family of curves I_D-V_{GS} for y_{film}=200nm, 10nm, 1nm, 0.3nm is presented. These curves have a maximum for $y_{film}\leq$1nm, like SET transistor, (Mahapatra, Ionescu, and Banerjee, 2002).

Figure 6.b shows the curves I_D-V_{DS} at V_{GS}=3V. The shape of the I_D-V_{DS} curves with a minimum proves the tunnel effect, accordingly with the equation (1).

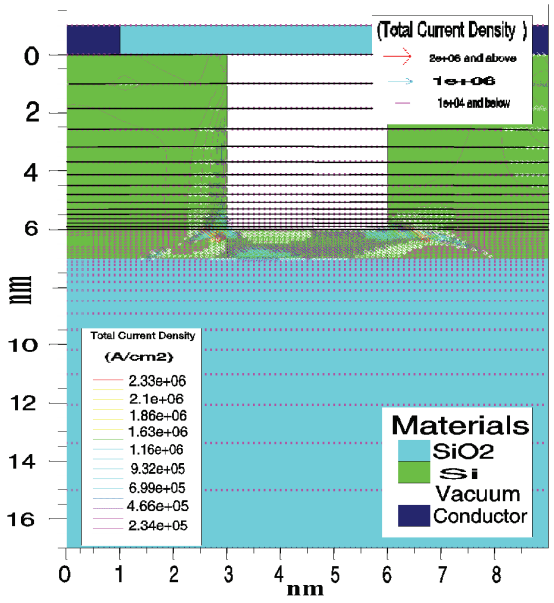


Figure 4: Total current vectors in the 1 nm transistor

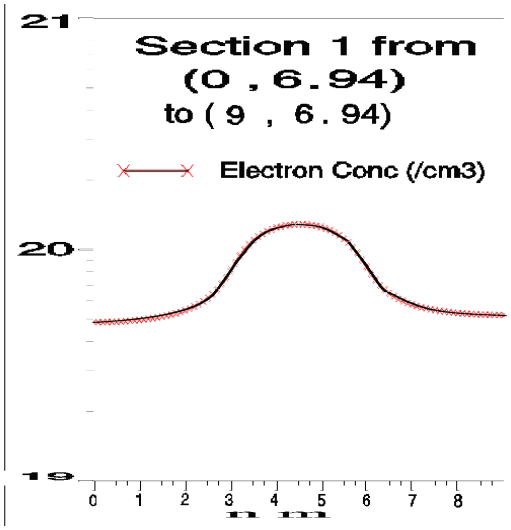
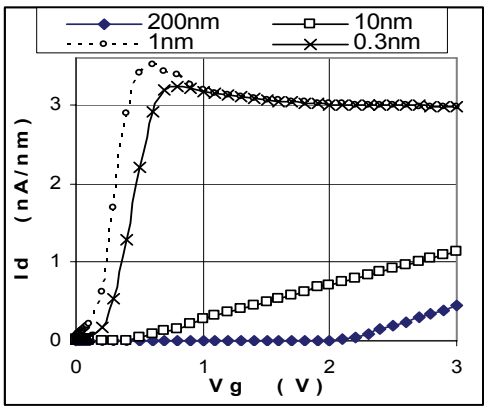
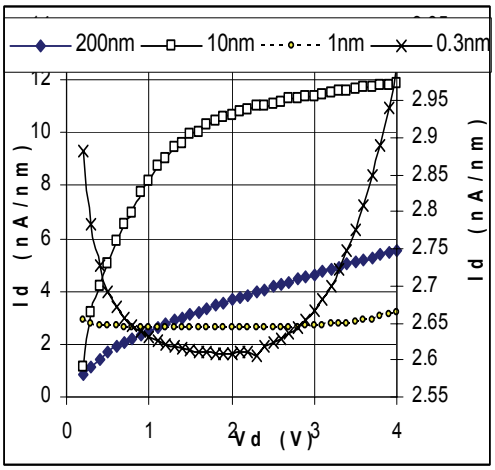


Figure 5: The electron concentrations in the 1nm transistor



(a)



(b)

Figure 6: (a) The I_D-V_{GS} ; (b) the I_D-V_{DS} , characteristics

Figure 7 presents the global potential distribution (left) and a detail of the electron concentration (right) for the 0.3nm structure with cavity, biased at a high drain voltage in this last case (V_S=0V, V_G=3V, V_D=4V).

In this case the saturation occurred and an unbalanced electron distribution can be seen in the film

(fig.7): $1.1 \cdot 10^{16}$ cm^{-3} in the source region, $7 \cdot 10^{15} cm^{-3}$ in the channel near the source, $2 \cdot 10^{15} cm^{-3}$ in the channel near the drain and decrease up to $1.4 \cdot 10^{15} cm^{-3}$ in the drain region, at the film bottom.

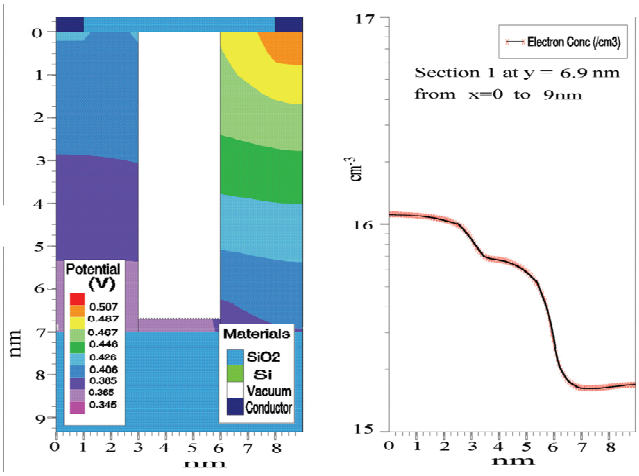


Figure 7: The potential and the electron concentration in the 0.3nm structure

6. CONCLUSIONS

A nanotransistor with Silicon On Insulator structure was presented. When the film thickness varied between 200nm to 10nm the electrical characteristics preserve the classical shape. When the film thickness varied from 1nm to 0.3nm and the cavity occurs above the film, the device presents atypical electrical characteristics I_D-V_{GS}, having a maximum like the SET transistor. The shape of the I_D-V_{DS} curves with a minimum proves the presence of the tunnel effect. The nanocavity comprises 1-3 air molecules in normal conditions, negligible for the current transport. Consequently doesn't imply a special vacuum technology. The electron transport in the p-film is one by one, proving the Single Electron Technology for our proposed SOI nanotransistor.

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